



Intel[®] Pentium[®] 4 Processor and Intel[®] E7205 Chipset

Platform Design Guide

*For Use with Intel[®] Pentium[®] 4 Processor with 512-KB L2 Cache on 0.13
Micron Process*

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Revision History

Revision	Description	Date
-001	Initial release.	November 2002
-002	Corrected incorrect RCOMP Values from 24.9 Ohms to 32.4 ohms	December 2002

Introduction

1

The *Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide* describes Intel's design recommendations for systems that are based on the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® E7205 chipset. The document provides motherboard design recommendations such as layout and routing guidelines, and addresses other system design issues such as power delivery. For specific design issues (e.g., thermal considerations), refer to the design guides and application notes listed in [Section 1.1](#), “[Reference Documentation](#)”.

In this document, “processor” and “chipset” refer to the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the E7205 chipset. Where a reference is intended to refer to a specific processor, the specific processor is listed.

The *Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide* has been developed to ensure maximum flexibility for board designers, while reducing board design risks. The design information provided in this document falls under one of the two following categories:

- *Design Recommendations.* These are items that are based on Intel's simulations and lab experience, are strongly recommended, and may be necessary to meet timing and signal quality specifications.
- *Design Considerations.* These are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel and should be used as examples, but may not be applicable to specific designs.

Note: The guidelines recommended in this document are based on experience, simulation, and validation work performed by Intel during development of Pentium 4 processors with 512-KB L2 cache on 0.13 micron process / E7205 chipset-based systems. This work is ongoing, and the recommendations are subject to change.

Platform schematics are included in [Appendix A](#). The schematics are for a specific design implementation, but the core schematics remain the same for most platforms that are based on the chipset. The schematic set provides a reference schematic for each chipset component, as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 Reference Documentation

Item	Location/Number
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet	298643
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines	http://developer.intel.com/design/Pentium4/guides/
Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Signal Integrity and Usage Guidelines	http://developer.intel.com/design/Pentium4/devtools/
Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478) Design Guidelines	http://www.intel.com/design/Pentium4/guides/249890.htm
Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet	249887
Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines	249889
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm
Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet	251937
Intel® E7205 and Intel® E7505 Length Matching Spreadsheet	Note 1
Intel® NetBurst™ Microarchitecture BIOS Writer's Guide	Note 1
Intel® Pentium® 4 Processor VR-Down Design Guidelines	Note 1
Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines	http://developer.intel.com/design/Xeon/guides
PCI Local Bus Specification	http://www.pcisig.com/
PCI-PCI Bridge Specification	http://www.pcisig.com/
PCI Bus Power Management Interface Specification	http://www.pcisig.com/
PCI-X Specification	http://www.pcisig.com/
PCI Local Bus Specification Rev 2.2	http://www.pcisig.com/
Serial ATA Specification Rev 1.0	http://www.serialata.org/cgi-bin/SerialATA10gold.zip
Sil3112 PCI to Serial ATA Controller Datasheet Rev 0.01	http://www.siliconimage.com/home.asp
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	http://www.intel.com/design/chipsets/datashts/290744.HTM
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions	http://www.intel.com/design/chipsets/applnots/292276.htm
JEDEC DDR SDRAM Unbuffered DIMM Design Specification	www.jedec.org
JEDEC DDR SDRAM Unbuffered DIMM Design Specification Addendum	http://www.intel.com/technology/memory/ddr/specs/ddr200_unbuff_dimm_spec_09.htm
JEDEC DDR SDRAM Registered DIMM Design Specification	http://www.intel.com/technology/memory/ddr/specs/ddr200_reg_dimm_spec_10.html
DDR200 JEDEC Specification Addendum	http://www.intel.com/technology/memory/pcsdram/spec/ddr200_spec_10.htm

Item	Location/Number
82562ET 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet	http://fdbl.intel.com/servlet/opencontentservlet?OBJID=09000d2980129c13
CK408 Clock Synthesizer/Driver Specification	Note 1
AC '97 Component Specification, Revision 2.3	http://developer.intel.com/ial/scalableplatforms/audio/
Communication and Network Riser Specification	http://developer.intel.com/technology/cnr/index.htm
ATA/ATAPI-6 Standard	http://T13.org
Intel® BGA/OLGA Assembly Development Guide- NDA r1.4	Note 1
Accelerated Graphics Port Interface Specification 3.0, Revision 0.95	http://www.agpforum.org/
Low Pin Count Interface Specification, Revision 1.0	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus 2.0 Specification	http://www.usb.org/
Advance Configuration and Power Interface (ACPI) Specification	http://www.teleport.com/~acpi/
Microsoft Windows* Logo Program System and Device Requirements	www.microsoft.com/hwdev/winlogo

NOTES:

1. Contact your Intel representative for the latest version of this item.

1.2 Terminology

This section defines conventions and terminology that is used throughout the design guide.

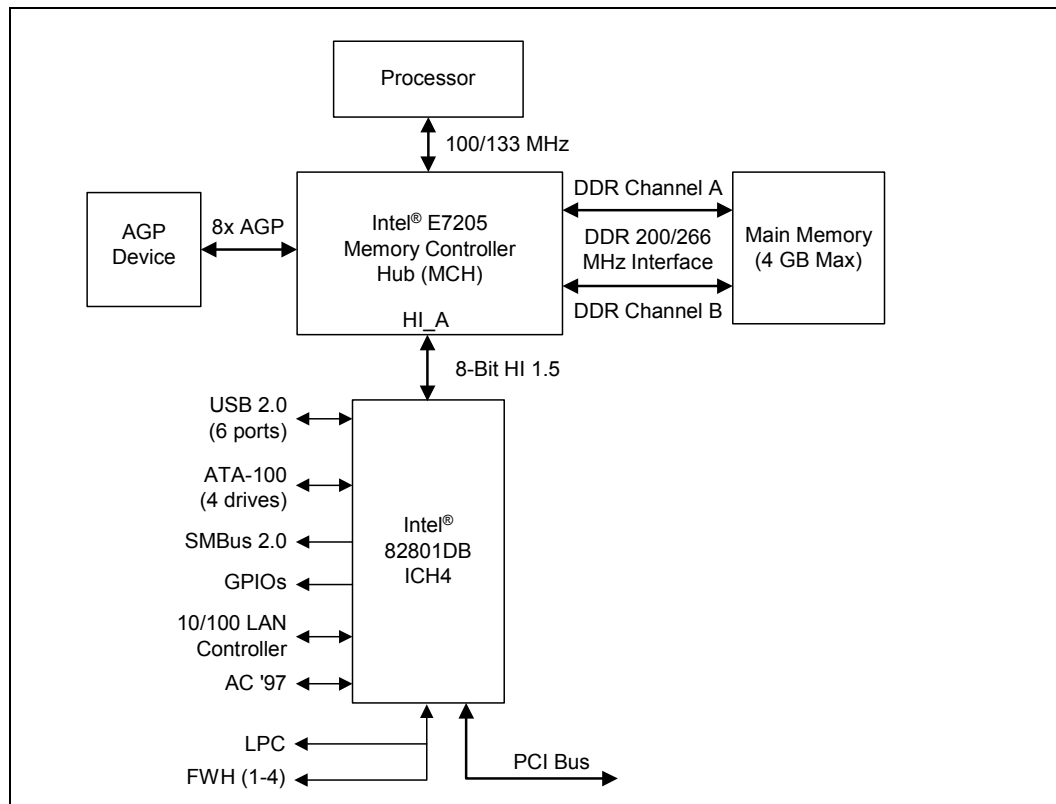
Term	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor's system buses use a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Pentium 4 processors with 512-KB L2 cache on 0.13 micron process do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SM#/, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to HCLKINP/HCLKINN. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two HCLKINs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	<p>The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.</p> <ul style="list-style-type: none"> Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flip Chip Ball Grid Array (FCBGA)	Microprocessor packaging using "flip chip" design, where the processor is attached to the substrate face-down for better signal integrity, more efficient heat removal and lower inductance.
Flight Time	<p>Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the Tco of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as:</p> <ul style="list-style-type: none"> The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. Maximum flight time is the largest acceptable flight time a network will experience under all conditions. Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.

Term	Description
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC_CPU.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	“Power-Good” or “PWRGOOD” (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage that a signal changes to after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the processor.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS that is observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The System Bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.3 System Overview

The E7205 chipset is designed for use with Pentium 4 processors with 512-KB L2 cache on 0.13 micron process. The architecture of the E7205 chipset provides the performance and feature-set required for single-processor based entry workstation system. [Figure 1-1](#) illustrates an example processor / chipset system configuration for entry workstation platforms.

Figure 1-1. Example Processor / Chipset Based System Configuration



1.3.1 Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is the next generation of the Pentium 4 processor in the 478-pin package with the Intel® NetBurst™ microarchitecture. The processor delivers performance levels that are significantly higher than previous generations of Intel® IA-32 processors. [Table 1-1](#) describes the basic feature set of the processor.

Table 1-1. Intel® Pentium® 4 Processor Feature Set Overview

Feature	Intel® Pentium® 4 Processor
L2 Cache	512-KB
Data Bus Transfer Rate	4.27 GB/s
Package	mPGA478

The processor includes the following advanced microarchitecture features:

- Advanced Dynamic Execution
- Execution Trace Cache
- Streaming SIMD (single instruction, multiple data) Extensions 2
- Advanced Transfer Cache
- Enhanced floating point and multimedia engine

1.3.2 Intel® E7205 Chipset

The chipset consists of two major components: the Memory Controller (MCH), and the I/O Controller 4 (ICH4). The chipset components communicate via the hub interface (HI).

The MCH is a 1005-ball FC-BGA package and contains the following functionality:

- System Bus Features:
 - Supports single processor at 533 MHz
 - System bus bandwidth of 4.27 GB/s
 - Supports 36-bit system bus addressing model
 - 12 deep in-order queue, 1-deep defer queue
- Memory Bus Features:
 - 144-bit wide, DDR266 (PC2100) memory interface Memory bandwidth of 4.27 GB/s or 3.2 GB/s.
 - Supports non-ECC (x64) and ECC (x72) DDR266 DIMMs using 128-Mb, 256-Mb, and 512-Mb DRAMs
 - Supports a maximum of 4 GB of memory
 - Supports S4EC/D4ED ECC
 - Supports up to 16 simultaneous open pages
- AGP 8X Bus Features
 - Single AGP device
 - AGP interface asynchronously coupled to core
 - AGP 3.0 Specification
 - 8X or 4X at 0.8 V (AGP 3.0) electrical characteristics
 - 4X, 2X, or 1X at 1.5 V (AGP 2.0) electrical characteristics
 - 0.8 V and 1.5 V AGP electrical. No 3.3 V support
 - 32-deep AGP request queue
 - 32-bit upstream address support for inbound AGP and PCI cycles
 - 32-bit downstream address support for outbound PCI and Fast Write cycles
- I/O Features
 - Provides HI1.5 Connection for ICH4
 - HI1.5 = HI1.0 protocols with HI2.0 electrical characteristics
 - 266 MB/s point-to-point connection for ICH4 with parity protection
 - 8-bit wide, 66 MHz base clock, 4X data transfer
 - Parallel termination mode for longer trace lengths
 - 64-bit inbound addressing, 32-bit outbound addressing

1.3.2.1 Intel® I/O Controller Hub 4 (ICH4)

The I/O Controller Hub (ICH4) provides the legacy I/O subsystem for E7205 chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH4 includes the following features:

- Provides H11.5 Connection to MCH
 - 266 MB/s point-to-point connection for ICH4 with parity protection
 - 8-bit wide, 66 MHz base clock, 4X data transfer
 - Parallel termination mode for longer trace lengths
 - 64-bit inbound addressing, 32-bit outbound addressing
- 2-channel Ultra ATA/100 bus master IDE controller
- 3 Universal Host Controller Interface (UHCI) USB host controllers (capabilities for six ports)
- I/O APIC
- SMBus 2.0 controller
- LPC interface
- AC '97 2.3 interface
- PCI 2.2 interface
- Integrated LAN Controller

1.3.3 Processor Support

Table 1-2 provides a summary of the supported processor configurations for the chipset-based platform.

Table 1-2. Supported Processor Configurations

Processor System Bus (MHz)	Installed Memory	Allowable	Comment
400	DDR200	Yes	Validated
400	DDR266	Yes	Validated
533	DDR200	No	Not validated
533	DDR266	Yes	Validated

1.3.4 DIMM Support

Table 1-3 provides a summary of the supported memory configurations for the chipset-based platform.

Table 1-3. DIMM Support Summary

Type	Unbuffered
Dual Channel	1 to 2 pairs of DIMMs (4 rows)

1.3.5 Bandwidth Summary

Table 1-4 describes the clock speed, sample rate, and bandwidth for each interface in the chipset-based platform.

Table 1-4. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus (Data)	133	4	8	4200
System Bus (Address)	133	2	4	1066
DDR Interface	133	2	16	4200
DDR Interface	100	2	16	3200
Hub Interface	66	4	1	266
AGP 8X	66	8	4	2032

Component Quadrant Layout

2

The quadrant layout figures below do not show the exact component ball count—only the general quadrant information. Use only the exact ball assignment to conduct a routing analysis. Reference the following documents for ball assignment information:

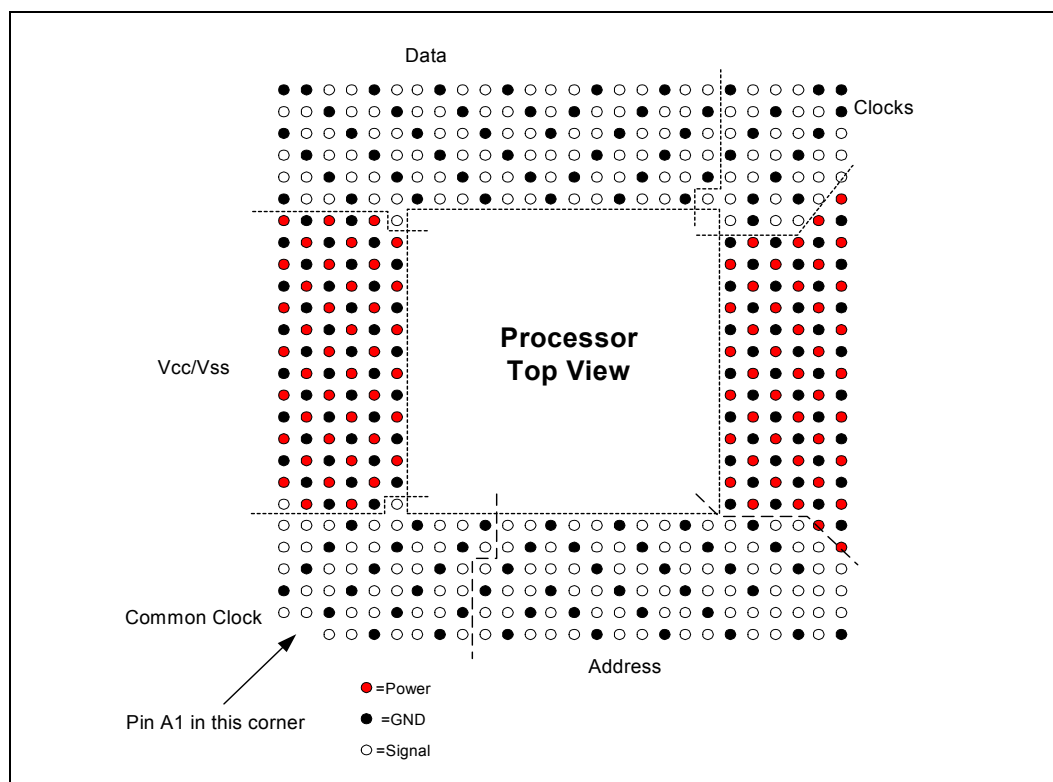
- *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet*
- *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet*
- *Intel® I/O Controller Hub 4 (ICH4) Datasheet*

Note: All figures in this section show the top view.

2.1 Intel® Pentium® 4 Processor Quadrant Layout

Figure 2-1 illustrates the quadrant layout of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

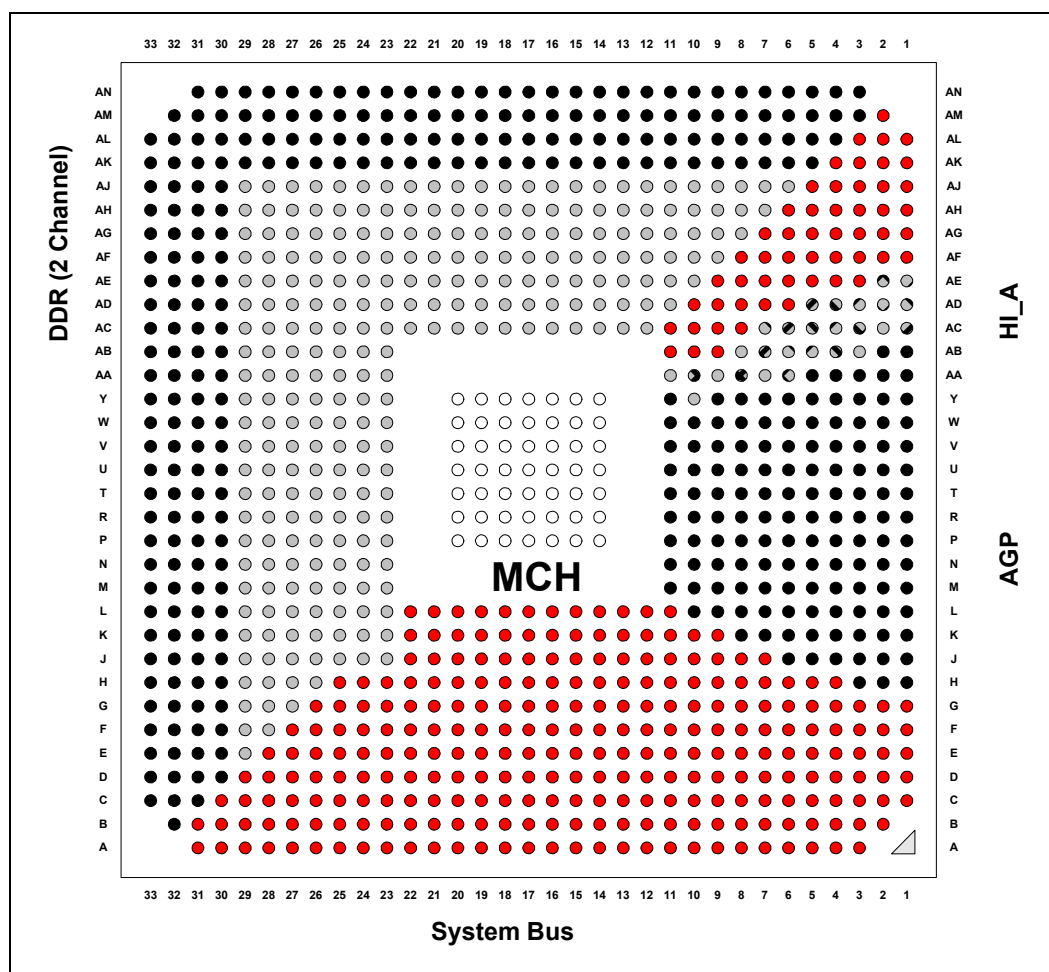
Figure 2-1. Intel® Pentium® 4 Processor Quadrant Layout (Top View)



2.2 MCH Quadrant Layout

Figure 2-2 illustrates the quadrant layout for the MCH chipset component.

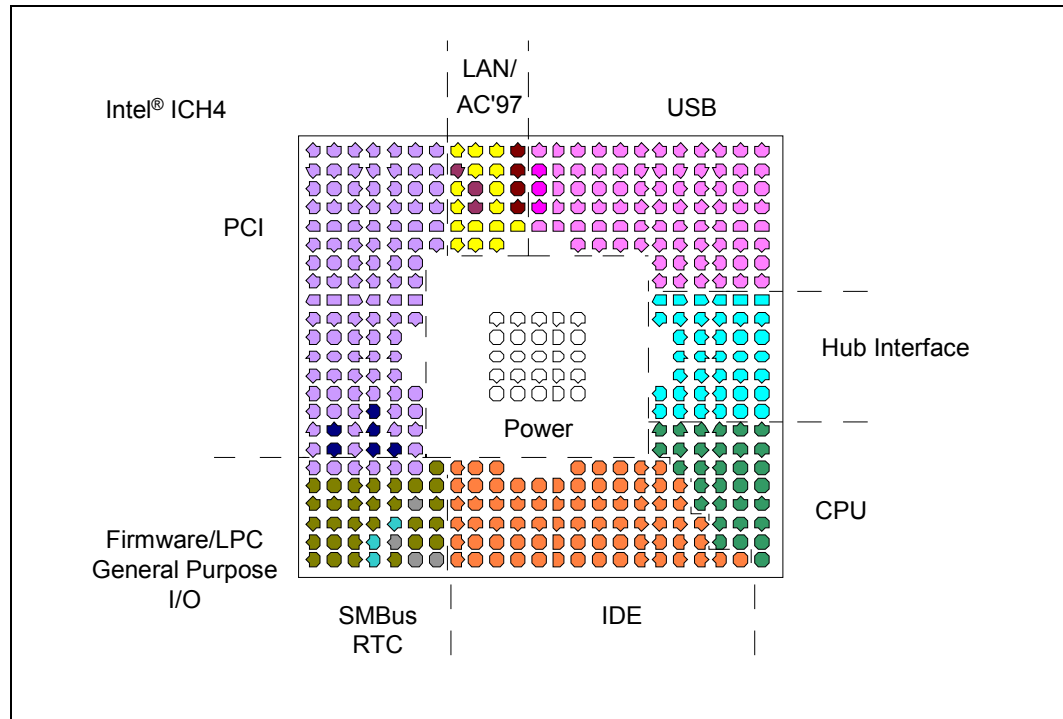
Figure 2-2. MCH Quadrant Layout (Top View)



2.3 Intel® ICH4 Quadrant Layout

Figure 2-3 shows the quadrant layout for the Intel® 82801CA ICH4 chipset component.

Figure 2-3. Intel® ICH4 Quadrant Layout (Top View)



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Platform Stack-Up and Component Placement Overview

3

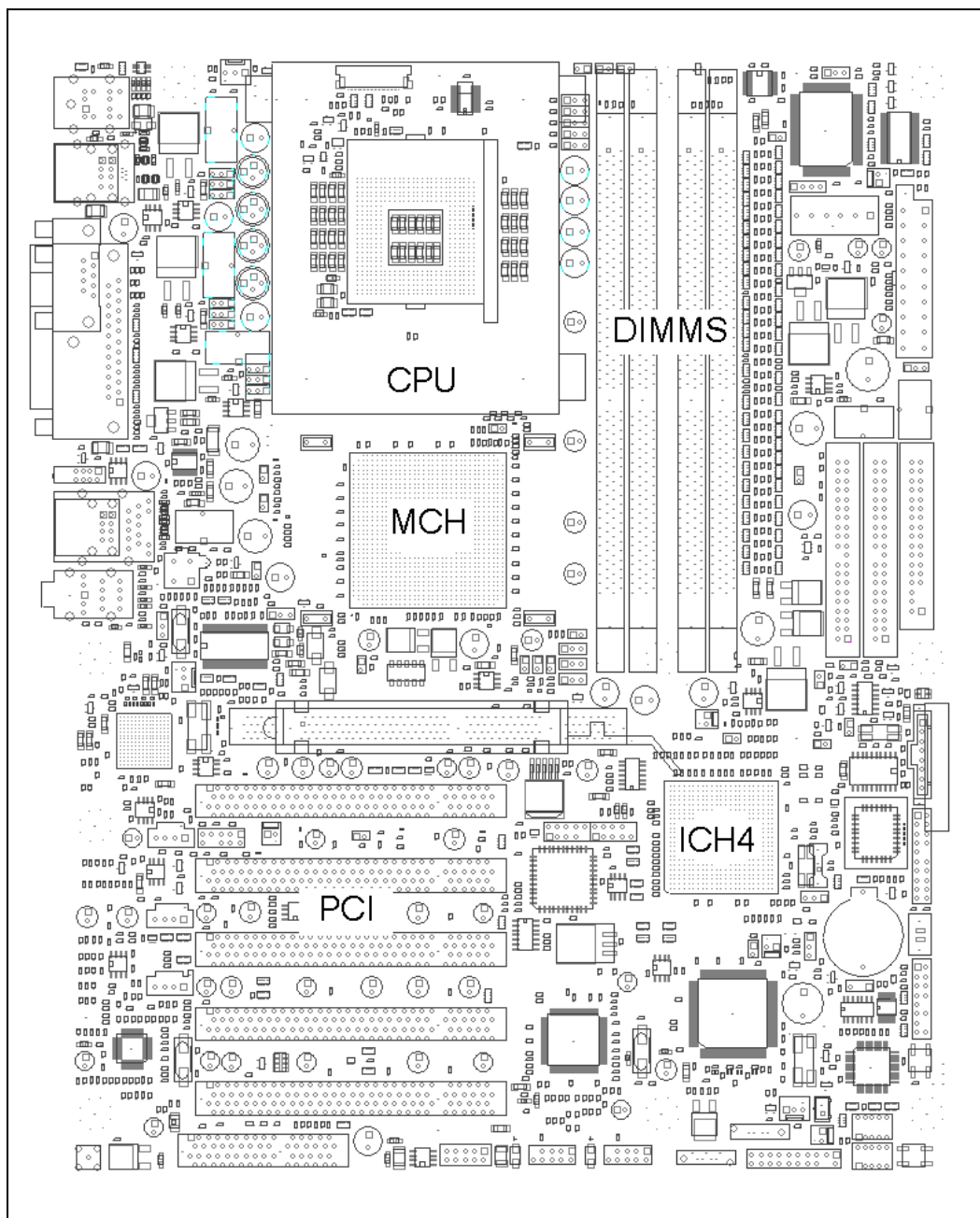
3.1 Platform Component Placement

Figure 3-1 illustrates the general component placement for the processor/chipset-based customer reference platform. Table 3-1 lists the assumptions used for the component placement.

Table 3-1. Assumptions for System Placement Example

System Configuration	Assumptions		
	Form Factor	Number of PCB Layers	Assembly
Entry Workstation (UP)	ATX (12" x 9.6")	6	Single Sided

Figure 3-1. Intel® Pentium® 4 Processor / Intel® E7205 Chipset-Based System Placement Example



3.2 Platform Stack-Up

Figure 3-2 shows the recommended platform stack-up. All internal layers are 1 oz. copper. Top and bottom layers are 0.5 oz. not including the plating. Because of the stackup, some signals will be routed stripline and/or microstrip. Layer 1, layer 4, and the bottom layer are used for signal routing with all three layers providing ground referencing.

Intel strongly recommends that system designers use the stack-up shown in Figure 3-2. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications will be met. This is particularly important if a design deviates from the design guidelines provided.

Figure 3-2. Board Stack-Up

		Layer Thickness	Copper Weight
Top	SIGNAL	2.1	0.5 oz plus plating
	PREPREG	4.0	
Layer 2	GND	1.2	1 oz.
	CORE	4.3	
Layer 3	POWER	1.2	1 oz.
	PREPREG	6.5	
	CORE	23.0	
Layer 4	PREPREG	6.5	
	SIGNAL	1.2	1 oz.
	CORE	4.3	
Layer 5	GND	1.2	1 oz.
	PREPREG	4.0	
Bottom	SIGNAL	2.1	0.5 oz plus plating
Panel Thickness (mils) =		61.6	Assumes finished thickness on μ Strip Layers



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Platform Clock Routing Guidelines 4

To minimize jitter, improve routing, and reduce cost, E7205 chipset-based systems will use a single-chip clock solution, the CK408. The CK408 provides three 133/100 MHz differential output pairs for all of the bus agents, and six 66 MHz speed clocks that drive all I/O buses. [Figure 4-1](#) shows the implementation of the bus clocks for this configuration. For more information on CK408, refer to the *CK408 Clock Synthesizer/Driver Specification*.

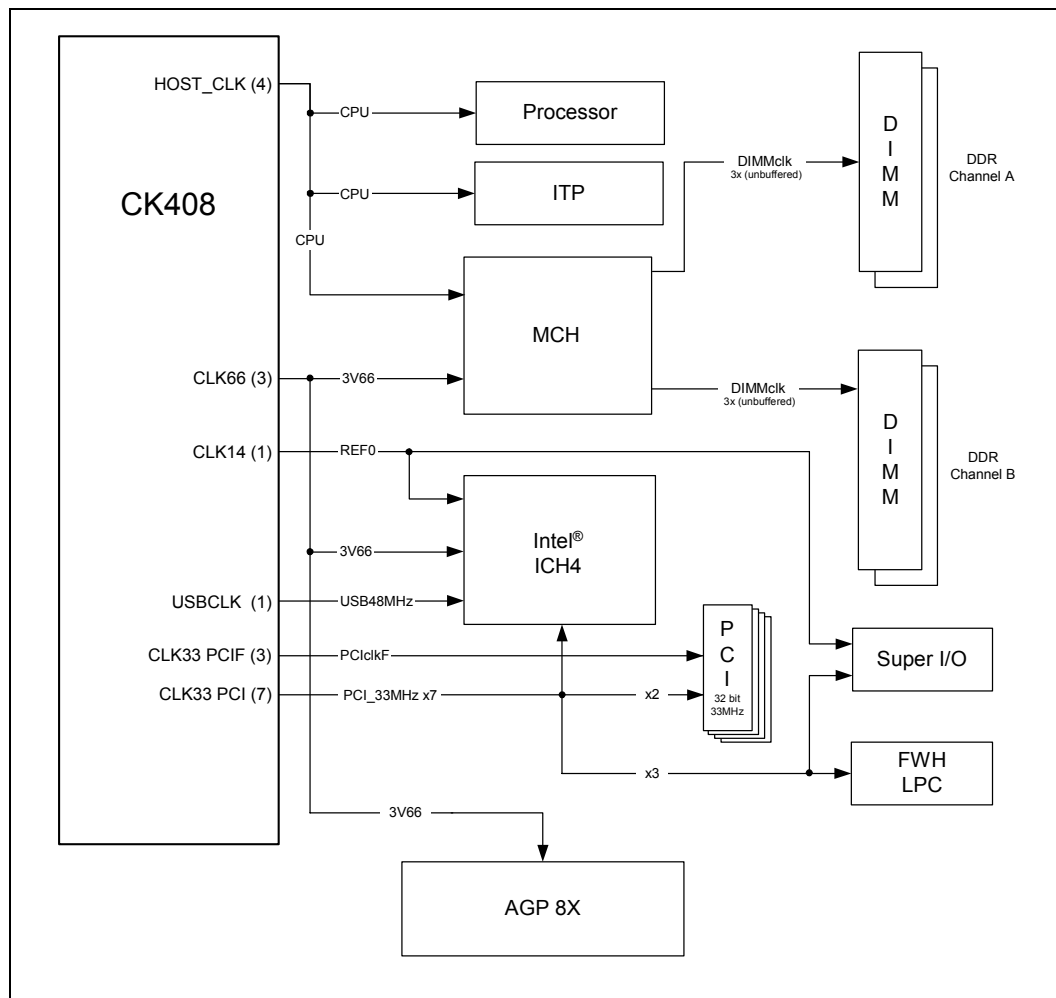
Table 4-1. Intel® E7205 Chipset Clock Group

Clock Name	Frequency (MHz)	Receiver
Host_CLK	133/100	Processor, MCH, Debug Port
CLK66	66	MCH, Intel® ICH4, AGP
CLK33	33	PCI Connector, ICH4, SIO, FWH
CLK14	14.318	ICH4, SIO
USBCLK	48	ICH4

Table 4-2. Platform System Clock Cross-Reference

Clock Group	CK-408	Component	Component Pin Name
HOST_CLK	CPU#	Debug Port	BCLK0
	CPU	Debug Port	BCLK1
	CPU#	Processor	BCLK0
	CPU	Processor	BCLK1
	CPU#	MCH	HCLKINN
	CPU	MCH	HCLKINP
CLK66	3V66_4	AGP	AGPCLK
	3V66_3	Port 80	N/A
	3V66_2	Intel® ICH4	CLK66
	3V66_1	MCH	GCLKIN
	3V66_0	Test Point	N/A
CLK33	PCI_33MHz	Slot 4	CLK
		Slot 5	CLK
		FWH. LPC	CLK, CLK
		SIO, Glue Chip	CLOCKI, CLK_IN
		SATA, 1394	PCI_CLK, PCI_PCLK
		LAN	P_CLK
		ICH4	PCICLK
	PCIClkF	Slot 3	CLK
		Slot 2	CLK
		Slot 1	CLK
CLK14	REF0	Audio	BIT_CLK
		ICH4	CLK14
		SIO	CLOCKI
USBCLK	USB48MHz	ICH4	CLK48

Figure 4-1. Intel® E7205 Chipset-Based System Clocking Diagram



4.1 Clock Groups

4.1.1 HOST_CLK Clock Group

4.1.1.1 HOST_CLK Clock Topology

The CK408 clock synthesizer provides three sets of 133/100 MHz differential clock outputs. The differential clocks are driven to the processors, the chipset, and the debug port as shown in Figure 4-1.

The clock driver differential bus output structure is a “Current Mode Current Steering” output, which develops a clock signal by alternately steering a programmable constant current to the external termination resistors, R_T . The resulting amplitude is determined by multiplying I_{OUT} by the value of R_T . The current I_{OUT} is programmable by a resistor and an internal multiplication factor so that the amplitude of the clock signal can be adjusted for different values of R_T to match impedances and to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to Figure 4-2 for an illustration of this termination method. Parallel R_T resistors perform a dual function—they convert the current output of the clock driver into a voltage, and they match the driver output impedance to the transmission line. The series resistors, R_S , provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor, R_T .

The value of R_T should be selected to match the characteristic impedance of the motherboard, and R_S should be between 20 Ω and 33 Ω . Simulations have shown that R_S values above 33 Ω provide no benefit to signal integrity and only degrade the edge rate.

Figure 4-2. Source Shunt Termination

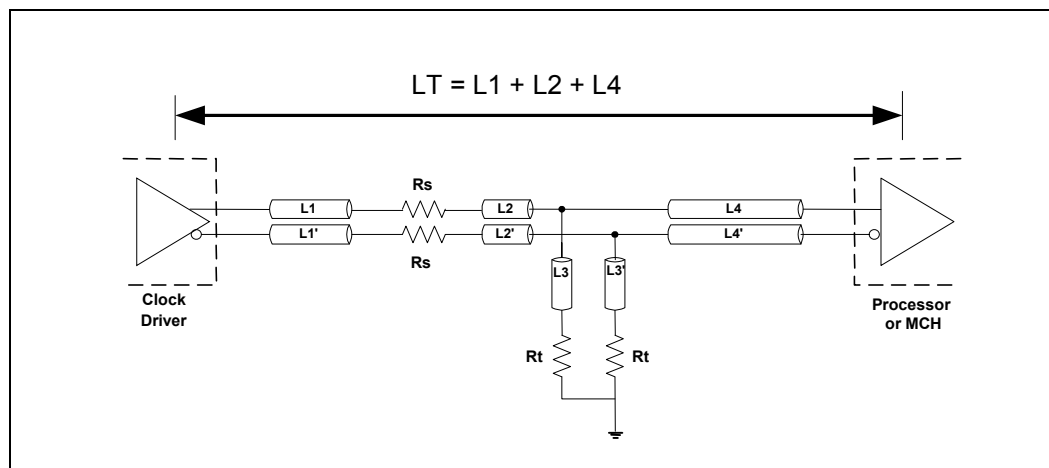


Table 4-3. HOST_CLK Routing Guidelines

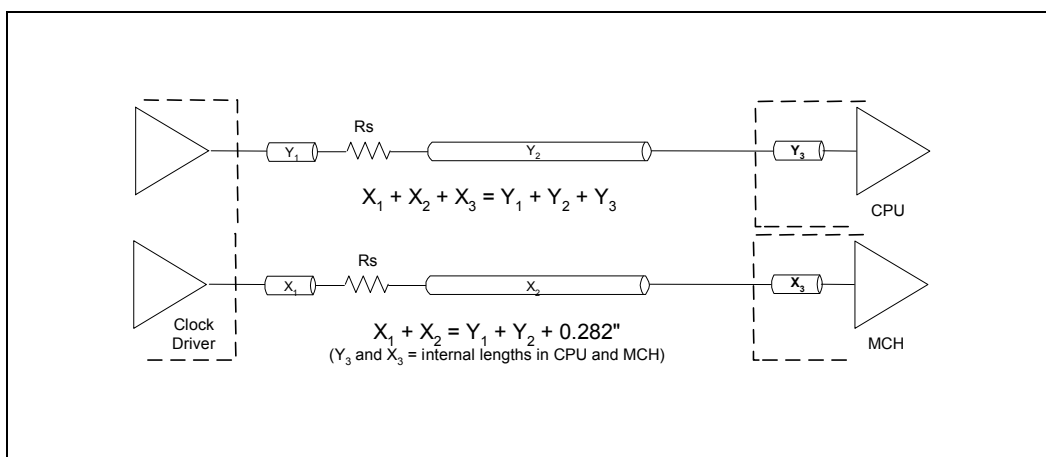
Layout Guideline	Value	Illustration	Notes
HCLKIN skew between agents	300 ps total Budget: 150 ps for clock driver 150 ps for interconnect	Figure 4-2 and Figure 4-4	1,2,3,4
Differential pair spacing	20 – 25 mils	Figure 4-5	5,6
Spacing to other traces	25 mils	Figure 4-5	
Serpentine spacing	Maintain a minimum S/h ratio of > 5/26 Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends, if possible.	Figure 4-5	
Motherboard impedance – differential	100 Ω typical		8
Motherboard impedance – single ended	50 $\Omega \pm 10\%$		9
Processor routing length – L1, L1': Clock driver to R _S	0.5 inch max	Figure 4-2	13
Processor routing length – L2, L2': R _S to R _S -R _T node	0 – 0.2 inch"	Figure 4-2	13
Processor routing length – L3, L3': R _S -R _T node to R _T	0 – 0.2 inch	Figure 4-2	13
Processor routing length – L4, L4': R _S -R _T Node to Load	0 – 10 inches	Figure 4-2	
MCH routing length – L1, L1': Clock Driver to R _S	0.5 inch max	Figure 4-2	13
MCH routing length – L2, L2': R _S to R _S -R _T node	0 – 0.2 inch	Figure 4-2	13
MCH routing length – L3, L3': R _S -R _T node to R _T	0 – 0.2 inch	Figure 4-2	13
MCH routing length – L4, L4': R _S -R _T Node to Load	0 – 10 inches	Figure 4-2	
Processor to CS length matching (LT)	0.282 inch \pm 0.010 inch Chipset LT must be 0.282 inch longer than Processor LT	Figure 4-2	10
Processor to processor length matching (LT)	\pm 10 mils	Figure 4-2	15
HCLKINP – HCLKINN length matching	\pm 10 mils		
R _S series termination value	33 $\Omega \pm 5\%$	Figure 4-2	11
R _T shunt termination value	49.9 $\Omega \pm 1\%$ (for 50 Ω MB impedance)	Figure 4-2	12

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes that clock pairs are routed on multiple routing layers and are routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.

5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
8. The differential impedance of each clock pair is approximately $2 \cdot Z_{\text{single-ended}} \cdot (1 - 2 \cdot K_b)$ where K_b is the backwards crosstalk coefficient. For the recommended trace spacing, K_b is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the HCLKIN traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the motherboard trace length for the chipset will be longer than the trace length for the processor.
11. R_s values between $20 \Omega - 33 \Omega$ have been shown to be effective.
12. R_t shunt termination value should match the motherboard impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination, and contribute to ring back.
14. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in E_r , and the impedance variations due to physical tolerances of circuit board material.
15. Length of LT for one processor must match the LT of all other HCLKIN traces to other processor with specific tolerance.

Figure 4-3. Length Matching of Host Clocks (with Package Compensation)



It's important that the host clocks from the clock pin to the processor silicon match the length from the clock pin to the MCH silicon. Package compensation is optional, but can be accommodated very easily.

The In-Target Probe clock lengths require a defined relationship to the processor and MCH host clock lengths. For more information on this relationship, refer to *ITP700 Debug Port Design Guide* (available at <http://www.intel.com/design/Xeon/guides/249679.htm>) for the design of your platform.

Figure 4-4. Clock Skew As Measured from Agent to Agent

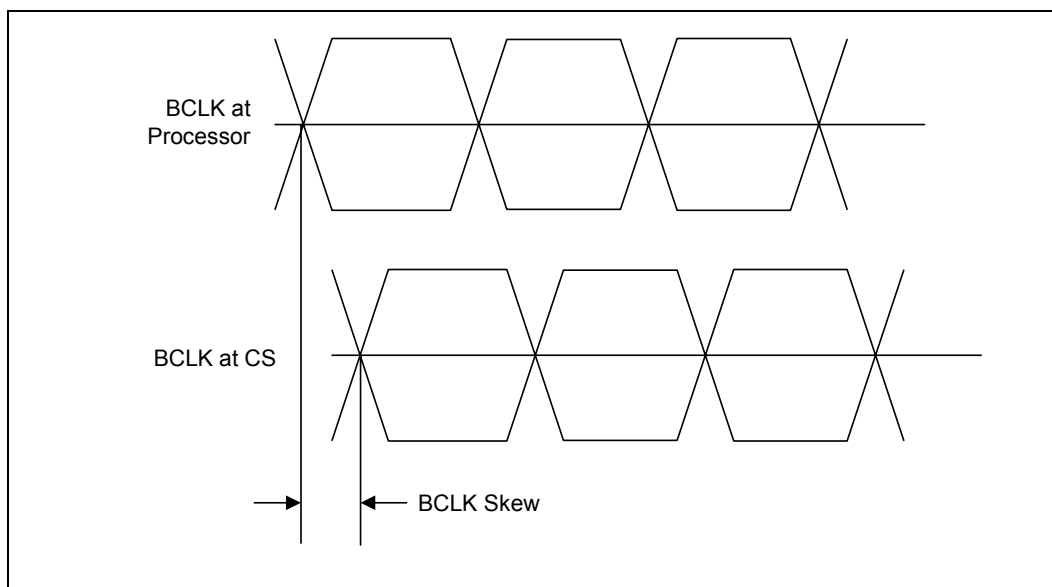
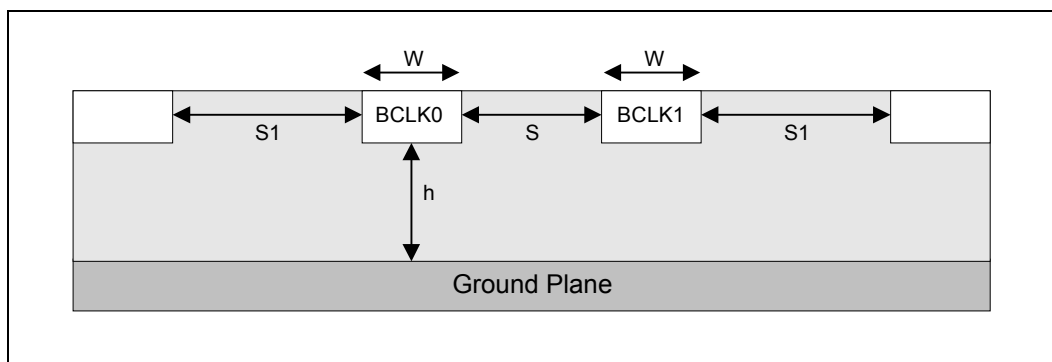


Figure 4-5. Trace Spacing



4.1.1.2 HOST_CLK General Routing Guidelines

- When routing the differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length $L1$, between clock driver and R_S , if needed to shorten length $L1$.

4.1.2 CLK66 Group

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH4, and AGP.

Figure 4-6. Topology for CLK66

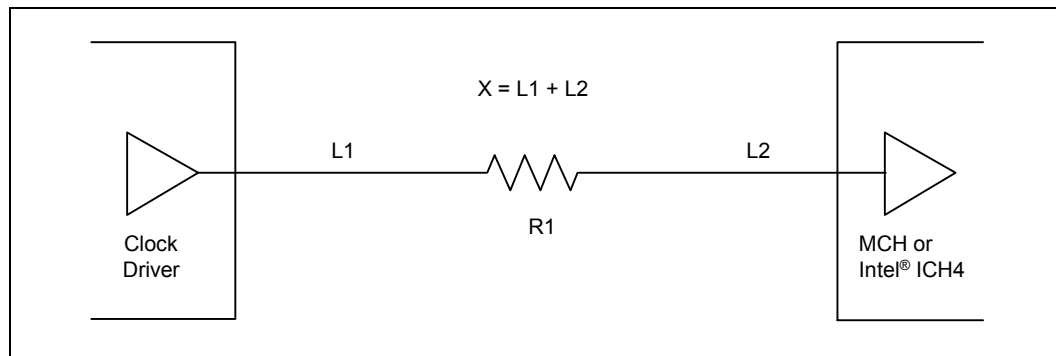


Table 4-4. CLK66 Routing Guidelines

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	$50 \Omega \pm 10\%$
Trace Width	6 mils on external layers, and 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 9.00 inches
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	The CLK66 group should minimize skew (~ 0) between each other.
Clock Driver to MCH	X (X can be between 3 inches– 9.5 inches)
Clock Driver to Intel® ICH4	X
Clock Driver to AGP connector	X – 4.6 inches (4 inches add-in card clock length plus 0.6 inch approximation for connector delay)

4.1.2.1 CLK66 Group to AGP Connector

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the AGP device. Use these guidelines when routing to an AGP connector.

Figure 4-7. Topology for CLK66 to AGP Connector

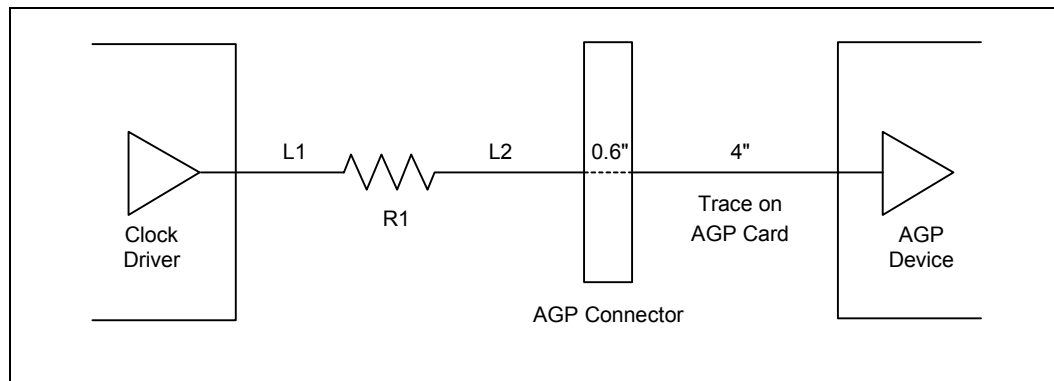


Table 4-5. CLK66 Routing Guidelines (for AGP Connector)

Parameters	Routing Guidelines
Topology	Point-to-point
Characteristic Trace Impedance (Z_0)	$50 \Omega \pm 10\%$
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	MCH 66 MHz Clock – L1 – 4.6 inches
AGPCLK Total Length (L1+L2)	MCH 66 MHz Clock – 4.6 inches (Must be matched to ± 100 mils of the CLK66 total length)
Resistor	$R1 = 33 \Omega \pm 5\%$

4.1.2.2 CLK66 Skew Requirements

All 66 MHz clock lengths require length matching. All devices down on the motherboard must have matching clock lengths. The AGP connector is equivalent approximately to 0.6 inch of trace, and 4 inches of clock trace exists on the add-in card. Therefore, the AGP clock is routed 4.6 inches shorter than the clocks to down devices (See Figure 4-8).

The skew between clocks can be further reduced by including the package lengths internal to the MCH and ICH4 in the length matching equations. This is not a requirement, but improves timing margins. Figure 4-9 shows the relationship between the 66 MHz clocks when accounting for internal package lengths.

Figure 4-8. Clock Skew and Tracing Requirements (Without Package Compensation)

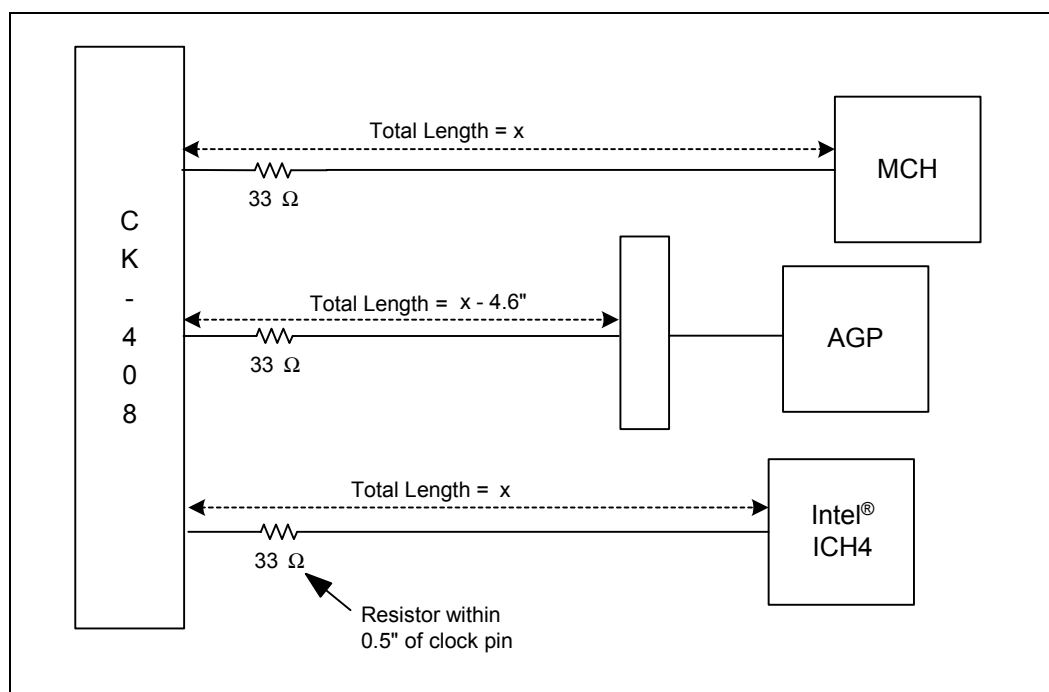
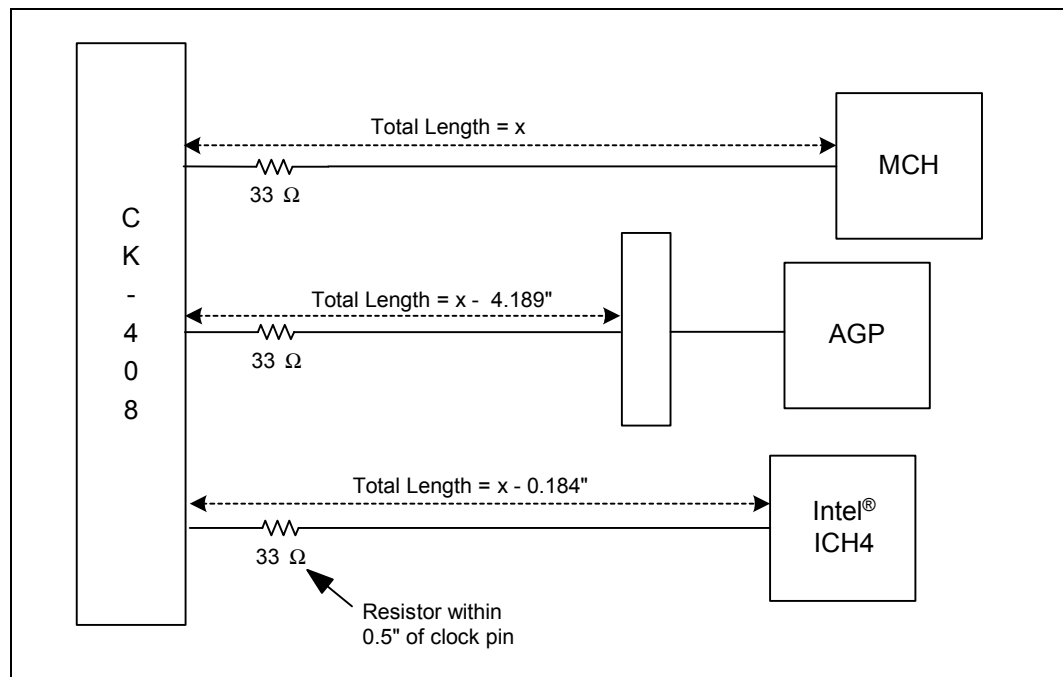


Figure 4-9. Clock Skew and Trace Requirements (With Package Compensation)



4.1.3 CLK33 Clock Group

The driver is the clock synthesizer's 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

Figure 4-10. Topology for CLK33 to PCI Device Down

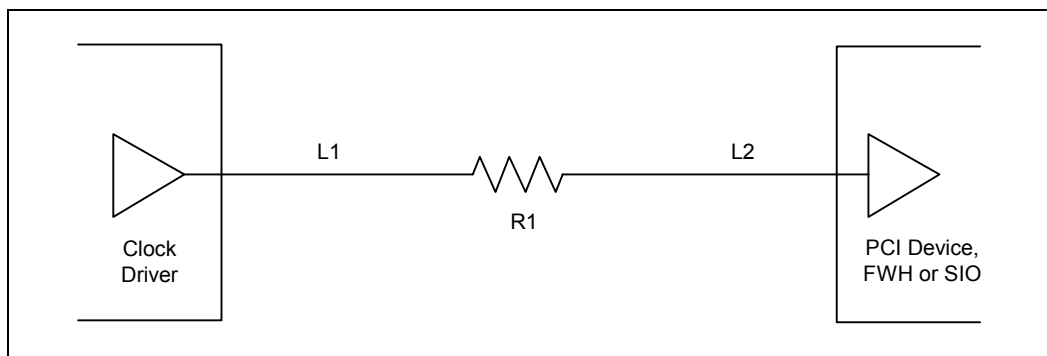


Table 4-6. CLK33 Routing Guidelines (PCI Device Down)

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	$50 \Omega \pm 10\%$
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1 ⁽¹⁾
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Spec is 2 ns. All PCI devices must be within 2 ns of Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore, up to ± 1 ns may be used to ease routing.

NOTES:

1. The 66 MHz total clock length must equal the 33 MHz total clock length, which is a requirement of the ICH4.
2. The designer must ensure that the total device to device skew on PCI bus does not exceed 2 ns including clock generator skew.

Figure 4-11. Topology for CLK33 to PCI Connector

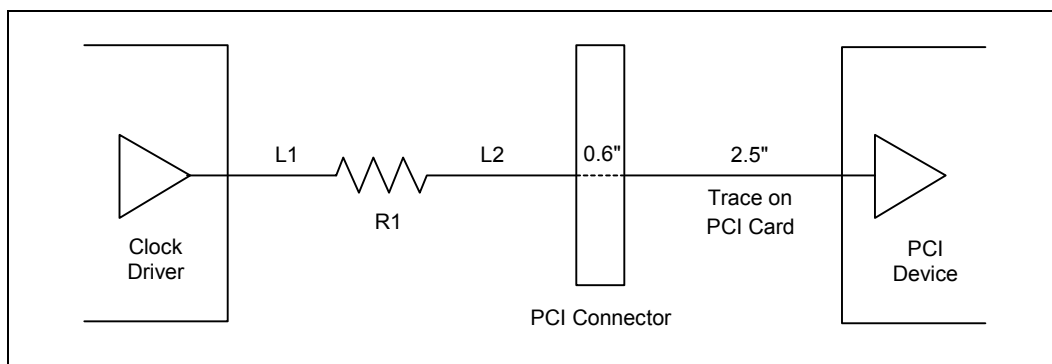


Table 4-7. CLK33 Routing Guidelines (for PCI Connector)

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point- to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	$50 \Omega \pm 10\%$
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1 – 3.1"
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Spec is 2 ns. All PCI devices must be within 2 ns of the Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore, up to ± 1 ns may be used to ease routing.

4.1.3.1 CLK33 Skew Requirements

All 33 MHz clocks to PCI devices must match in length. In addition, the 33 MHz clock to the ICH4 must match the length of the 66 MHz clock to the ICH4. The PCI connector is equivalent to approximately 0.6 inch of trace, and 2.5 inches of clock trace exists on the add-in card. Therefore, the clock to PCI slots is required to be 3.1 inches shorter than the clocks to down devices to ensure that the length from the clock chip to all PCI devices is equal.

The skew between clocks can be further improved by including the package lengths internal to the MCH and ICH4. This is not a requirement, but improves timing margins. [Figure 4-13](#) shows the relationship between the 33 MHz clocks when accounting for internal package lengths.

Figure 4-12. Clock Skew and Tracing Requirements (Without Package Compensation)

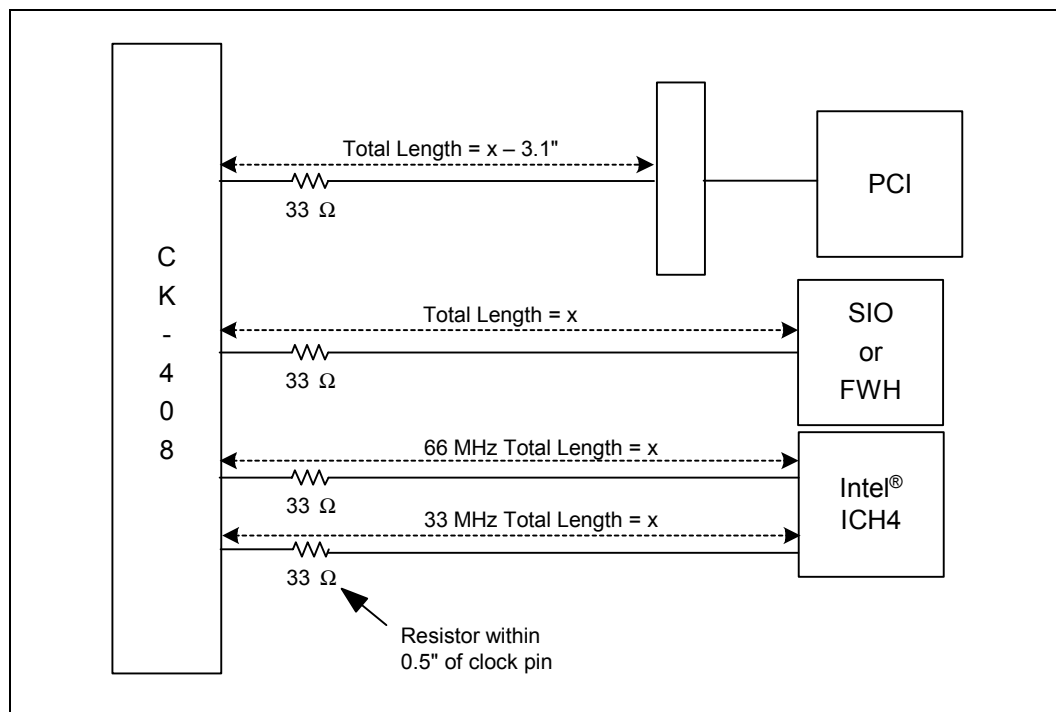
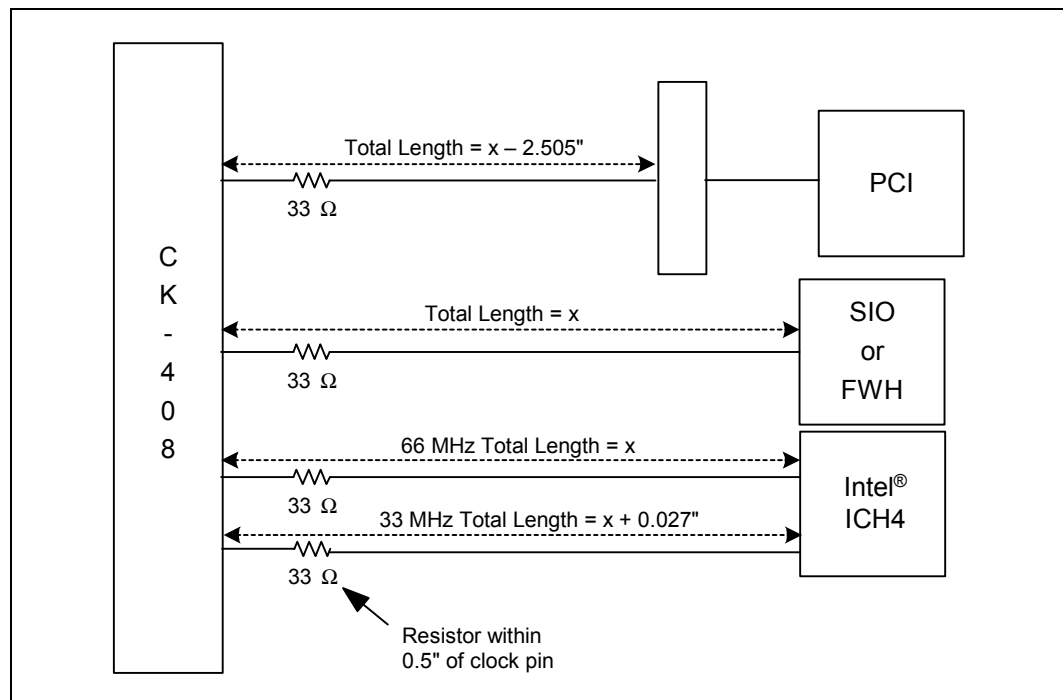


Figure 4-13. Clock Skew and Trace Requirements (With Package Compensation)



4.1.4 CLK14 Clock Group

The driver is the clock synthesizer's 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO.

Figure 4-14. Topology for CLK14

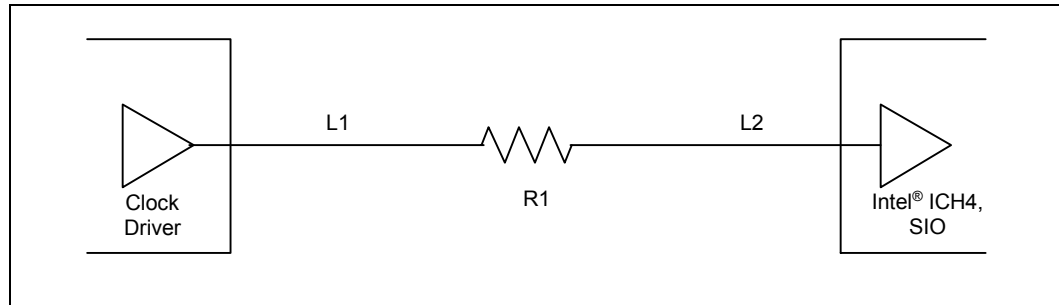


Table 4-8. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 $\Omega \pm 10\%$
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50"
Trace Length – L2	3.00 – 9.00"
Resistor	R1 = 33 $\Omega \pm 5\%$
Skew Requirements	Should have minimal skew (~ 0) between each other. However, each of the clocks in this group is asynchronous to clocks of any other group.

4.1.5 USBCLK Clock Group

The driver is the clock synthesizer's USB clock output buffer, and the receiver is the USB clock input buffer at the ICH4.

Figure 4-15. Topology for USB_CLK

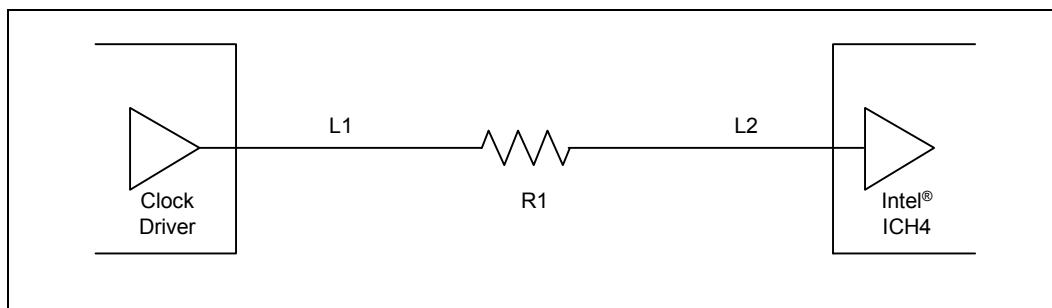


Table 4-9. USBCLK Routing Guidelines

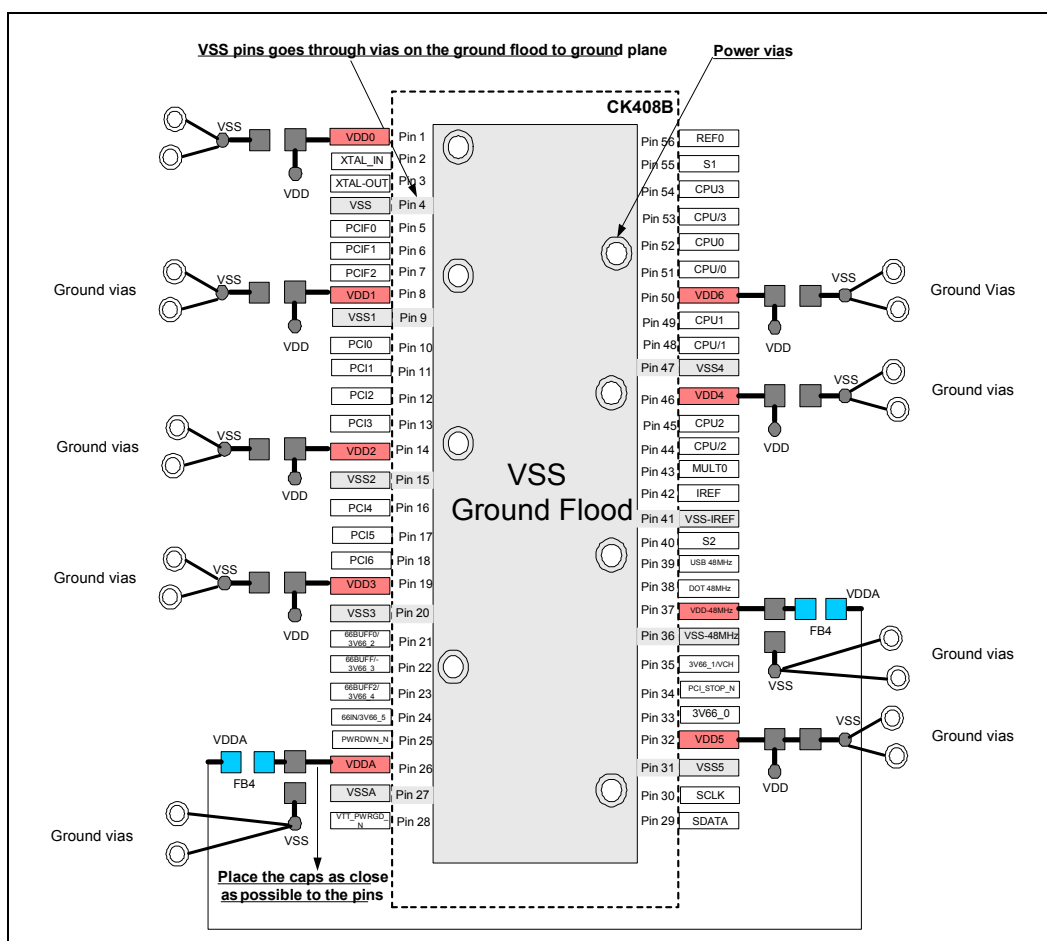
Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	$50\ \Omega \pm 10\%$
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 12.00 inches
Resistor	$R1 = 33\ \Omega \pm 5\%$
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board.
Maximum Via Count per Signal	2

4.2 Clock Driver Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One 22 μF polarized (decoupling) cap placed close to the V_{DD} generation circuitry.
- Eleven 0.1 μF high-frequency decoupling caps placed close to the V_{DD} pins on the Clock driver.
- Three 0.1 μF high-frequency decoupling caps placed close to the V_{DDA} pins on the Clock driver.
- One 10 μF polarized (decoupling) cap placed close to the V_{DDA} pins on the Clock driver.
- One 0.1 μF high-frequency decoupling cap placed close to the V_{DDA} generation circuitry.
- All decoupling caps should be placed close to the Clock driver pins. Refer to [Figure 4-16](#).

Figure 4-16. Decoupling Capacitors Placement and Connectivity



4.3 Clock Driver Power Delivery

Special care must be taken to provide a quiet V_{DDA} supply to the Ref V_{DD} , V_{DDA} and the 48 MHz V_{DD} . These V_{DDA} signals are especially sensitive to switching noise induced by the other V_{DD} s on the clock chip. They are also sensitive to switching noise generated elsewhere in the system, such as CPU VRM. It is recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling caps, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.

4.4 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to a VSS reference plane only.



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System Bus Routing Guidelines

5

5.1 Processor System Bus Guidelines

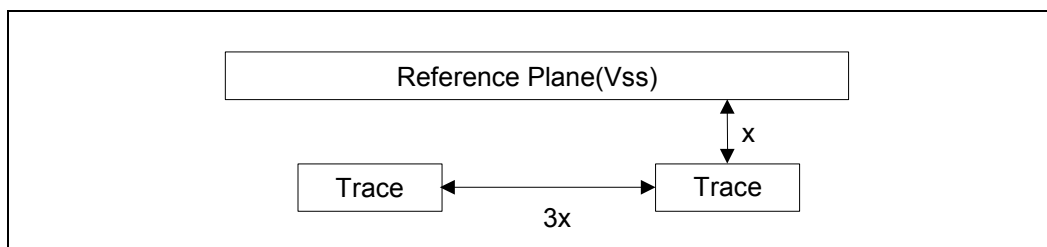
This section covers the system bus source synchronous (data, address, and associated strobes) and common clock signal routing for systems. [Table 5-1](#) summarizes the layout recommendations for Pentium 4 processors with 512-KB L2 cache on 0.13 micron process configurations, and expands on specific design issues and their recommendations.

Table 5-1. System Bus Routing Summary for the Processor¹

Parameter	Type
Line-to-Line Spacing ²	Data and common clock system bus must be routed at 7-mil wide traces and with 13-mil spacing
Breakout Guidelines (Processor and MCH)	7-mil wide with 5-mil spacing for a maximum of 250 mils from the component ball
Data Line Lengths (agent to agent spacing)	2"– 10" from pin to pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS.
DSTBn/p[3:0]#	A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length. If one strobe switches layers, its complement must switch layers in the same manner. DSTBn/p# should be referenced to VSS
Address Line Lengths (agent to agent spacing) ADSTB[1:0]#	2" – 10" from pin to pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).
Common Clock Line Lengths	2.5" – 10" pin to pin. No length compensation is necessary.
Topology	Point-to-point (chipset to processor).
Routing Priorities	All signals should be referenced to VSS. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example). The Data Bus must be routed first, then the address bus and then common clock.
Clock keep-Out Zones	Refer to Table 4-3 .
Trace Impedance	50 $\Omega \pm 15\%$

NOTES:

1. Refer to the *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet* for MCH package dimensions, and refer to the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Signal Integrity and Usage Guidelines* for processor package dimensions.
2. Data and common clock system bus may be routed at 7 mil wide traces and with 10 mil spacing if line length is kept under 6 inches.

Figure 5-1. Cross-Sectional View of 3:1 Ratio

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, and vias, VRMs etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

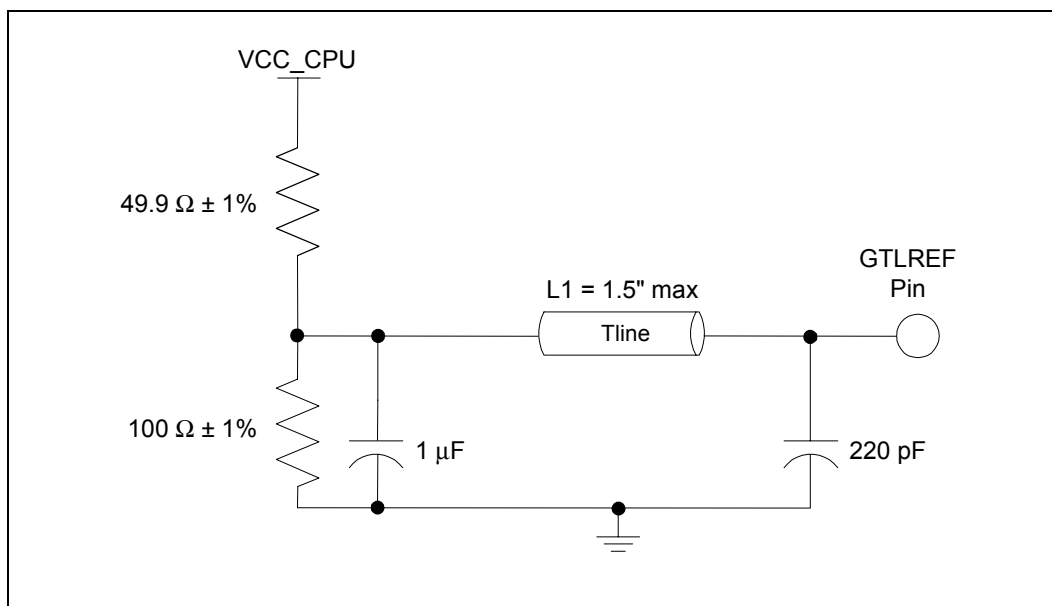
The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain VSS as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

5.2 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage may be supplied to only one of the four pins.

Figure 5-2. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 μ F capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin
- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7-mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the System Bus signals.)

5.2.1 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the MCH

The HVREF signals must be tied to a resistor divider network that supplies $2/3 \cdot VCC_CPU$. Use one $49.9 \Omega \pm 1\%$ resistor to the VCC_CPU plane, and one $100 \Omega \pm 1\%$ resistor to ground for the divider. Decouple with one $0.1 \mu F$ capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies $1/3 \cdot VCC_CPU$. Use one $300 \Omega \pm 1\%$ resistor to the VCC_CPU plane, and one $150 \Omega \pm 1\%$ resistor to ground for the divider. Decouple with one $0.01 \mu F$ capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at least 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a $32.4 \Omega \pm 1\%$ resistor. The trace to each resistor should be routed a maximum of 0.5 inches at 10 mils wide. Keep each trace at least 7 mils away from other signals.

5.3 Processor Configuration

5.3.1 Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Configuration

This section provides more details for routing Pentium 4 processors with 512-KB L2 cache on 0.13 micron process-based systems. Both recommendations and considerations are presented.

For proper operation of the processor and chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions that may not apply to specific OEM system designs. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet* for a system bus signal list, a description of signal types, and signal definitions.

5.3.2 Topology and Routing

Table 5-2. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

5.3.2.1 Design Recommendations

The following are the design recommendations for the data, address, data strobes, and common clock signals. Based on the example shown in [Figure 5-3](#), the data, address, strobe and common clock should be routed 7 mils with 13 mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

Data

The pin-to-pin distance for the data signals from the processor to the chipset should be between 2.0 inches and 10 inches (i.e., $2.0" < L1 < 10"$). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace will be added to some data nets on the system board so that all trace lengths within the same data group are the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains VSS.

$$\text{delta}_{\text{net,strobe}} = (\text{cpu_pkglen}_{\text{net}} - \text{cpu_pkglen}_{\text{strobe}}) + (\text{cs_pkglen}_{\text{net}} - \text{cs_pkglen}_{\text{strobe}})$$

Equation 5-1. Calculation to Determine Package Delta Addition to Motherboard Length for UP Systems

Note: Refer to *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet* for package lengths.

Note: Strobe package length is the average of the strobe pair.

Address

Address signals follow the same rules as data signals with the exception that they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains VSS.

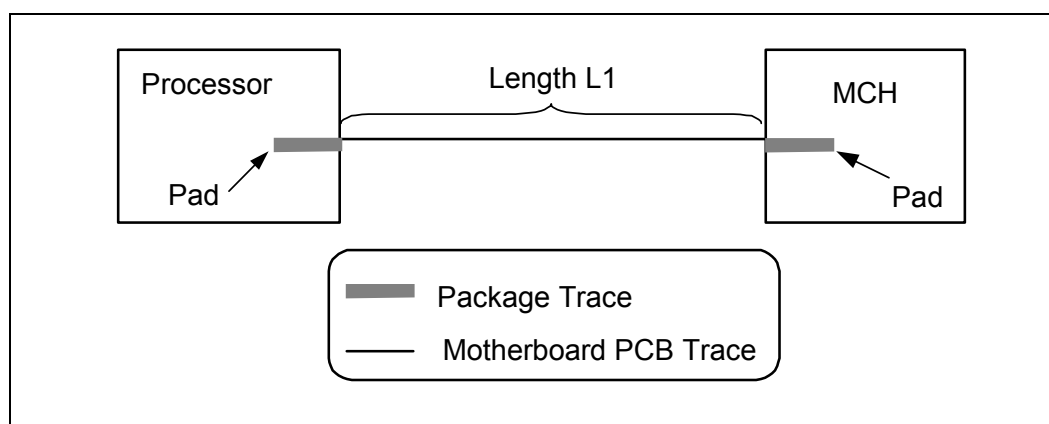
Data Strobes

A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ± 25 mils of the same length. It is recommended that skew be simulated to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 2.5 inches, and a maximum motherboard length of 10 inches.

Figure 5-3. Processor Topology



5.4 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobes and address. Table 5-3 lists the signals that are described in this section.

Table 5-3. Miscellaneous Signals (Signals That Are Not Data, Address, or Strobe)

Signal Name	Type	Direction	Topology	Driven by
A20M#	Asynchronous GTL+	I	2	Intel® ICH4
BR0#	AGTL+	I/O	4	Processor
XCOMP/YCOMP	Analog	I	5	
FERR#	Asynchronous GTL+ Open Drain	O	1	Processor
IGNNE#	Asynchronous GTL+	I	2	ICH4
INIT#	Asynchronous GTL+	I	2-A	ICH4
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2	ICH4
PROCHOT#	Asynchronous GTL+ Open Drain	O	1	Processor
PWRGOOD	Other	I	2-B	ICH4
RESET#	AGTL+ Open Drain	I	4	MCH
SLP#	Asynchronous GTL+	I	2	ICH4
SMI#	Asynchronous GTL+	I	2	ICH4
STPCLK#	Asynchronous GTL+	I	2	ICH4
THERMTRIP#	AGTL+ Open Drain	O	1	Processor
VCCA	Power	I	3	External logic
VCCIOPLL	Power	I	3	External logic
VCC_SENSE	Other	O		Processor
VCCVID[4:0]	Open Drain 3.3 V Tolerant	O	8, 9	Processor
VSSA	Power	I	3	Ground
THERMDA/ THERMDC	Other	I/O	6	External logic
TESTHI	Other	I/O	7	External logic

All signals must meet the AC and DC specifications described in the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet*.

5.4.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

5.4.1.1 Topology 1: Asynchronous GTL+ Signals Driven by the Processor—FERR#, PROCHOT# and THERMTRIP#

These signals should adhere to the following routing and layout recommendations. Figure 5-4 illustrates the recommended topology. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 5-4. Layout Recommendations for FERR# and THERMTRIP# Signals—Topology 1

Trace Z_0	Trace Spacing	L1	L3	R_{PU}
50 Ω	7 mil	1" – 12"	3" max	62 \pm 5% Ω

Figure 5-4. Routing Illustration for FERR# and THERMTRIP#

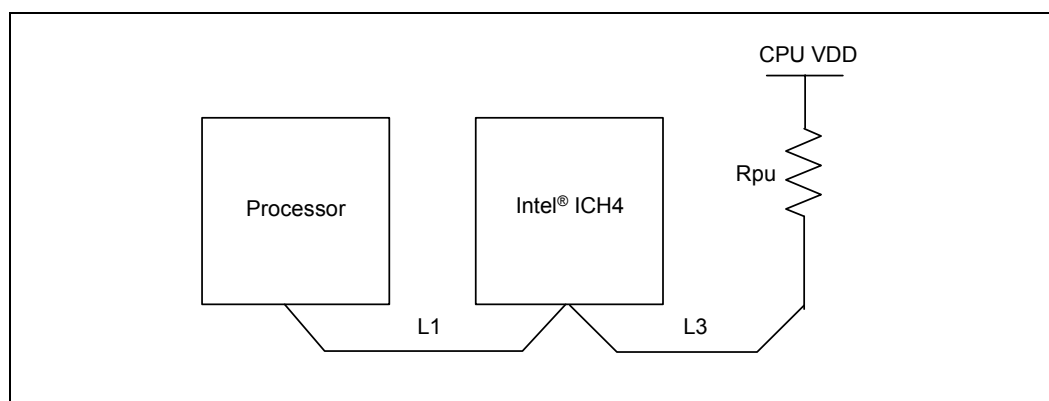
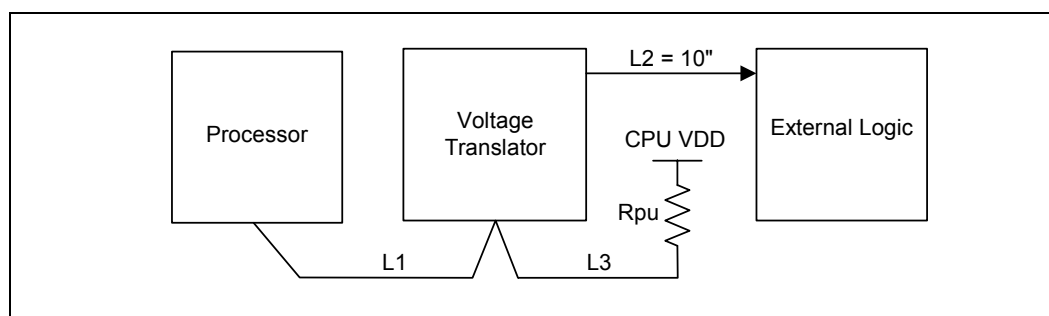


Table 5-5. Layout Recommendations for PROCHOT# Signal—Topology 1

Trace Z_0	Trace Spacing	L1	L2	L3	R_{PU}
50 Ω	7 mil	1" – 17"	10" max	3" max	62 \pm 5% Ω

Figure 5-5. Routing Illustration for PROCHOT#



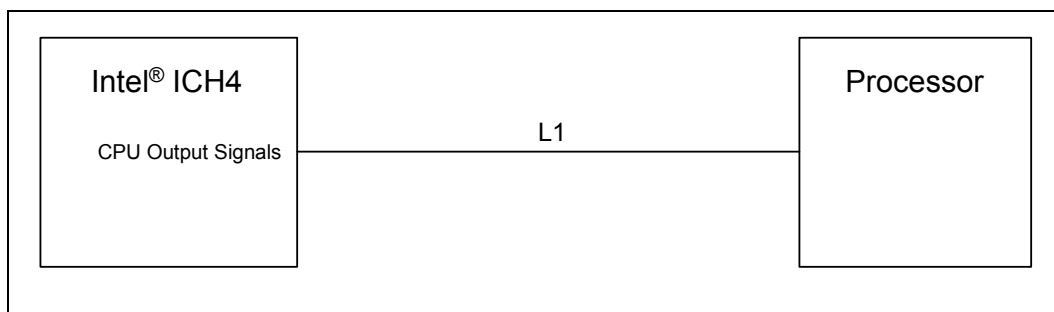
5.4.1.2 Topology 2: Asynchronous GTL+ Signals Driven by the Intel® ICH4—A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

The V_CPU_IO signals are documented to support only 0.8 V to 1.75 V. The ICH4 output signals voltage swing depend on the voltage passed into these signals (V_CPU_IO[2:0]), and voltages below 0.8 V are not supported by the ICH4's buffers. These signals should adhere to the following routing and layout recommendations. Figure 5-6 illustrates the recommended topology.

Table 5-6. Layout Recommendations for Miscellaneous Signals—Topology 2

Processor CMOS Routing Requirements	Maximum Trace Length	Signal Referencing	Processor CMOS Signals Length Matching
5 on 5	L1 = 19 inches	N/A	None

Figure 5-6. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#



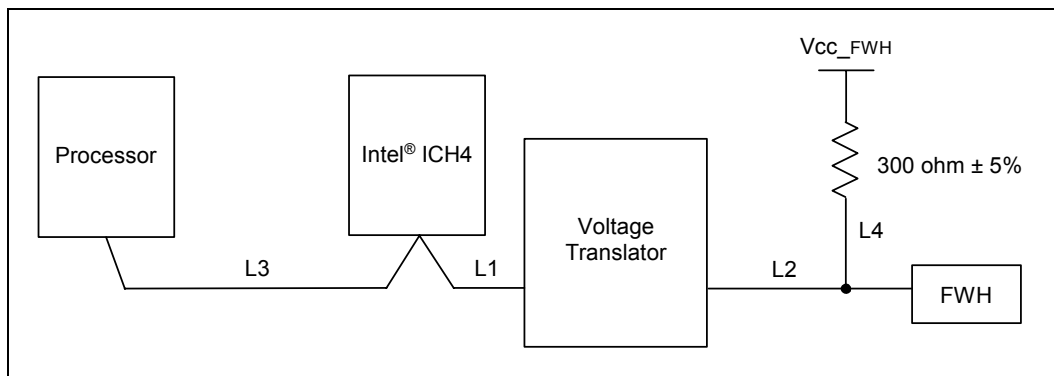
5.4.1.3 Topology 2-A: INIT#

Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. See Section 10.4.4 for voltage level translation circuitry.

Table 5-7. Layout Recommendations for INIT#—Topology 2A

Trace Z ₀	Trace Spacing	L1	L2	L3	L4	R _{PU}
50 Ω	7 mil	2" max	10" max	17" max	3" max	300 Ω ± 5%

Figure 5-7. Routing Illustration for INIT#



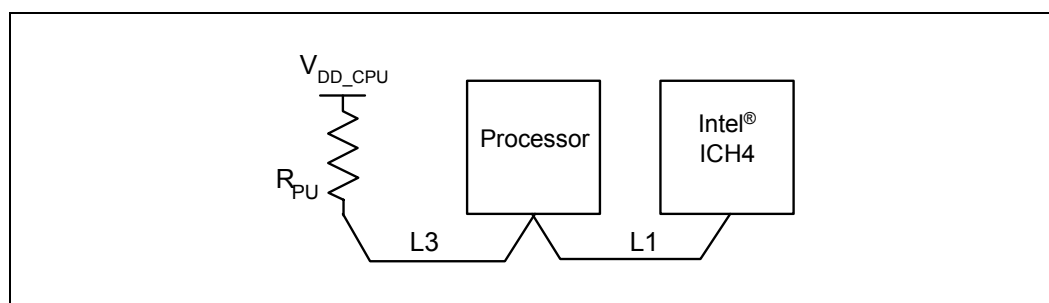
5.4.1.4 Topology 2-B: Miscellaneous Signals Driven by the Intel® ICH4 Open Drain; PWRGOOD

This signal should adhere to the following routing and layout recommendations. [Figure 5-8](#) illustrates the recommended topology.

Table 5-8. Layout Recommendations for Miscellaneous Signals—Topology 2B

Trace Z_0	Trace Spacing	L1	L3	R_{PU}
50 Ω	7 mil	1" – 12"	3" max	300 $\Omega \pm 5\%$

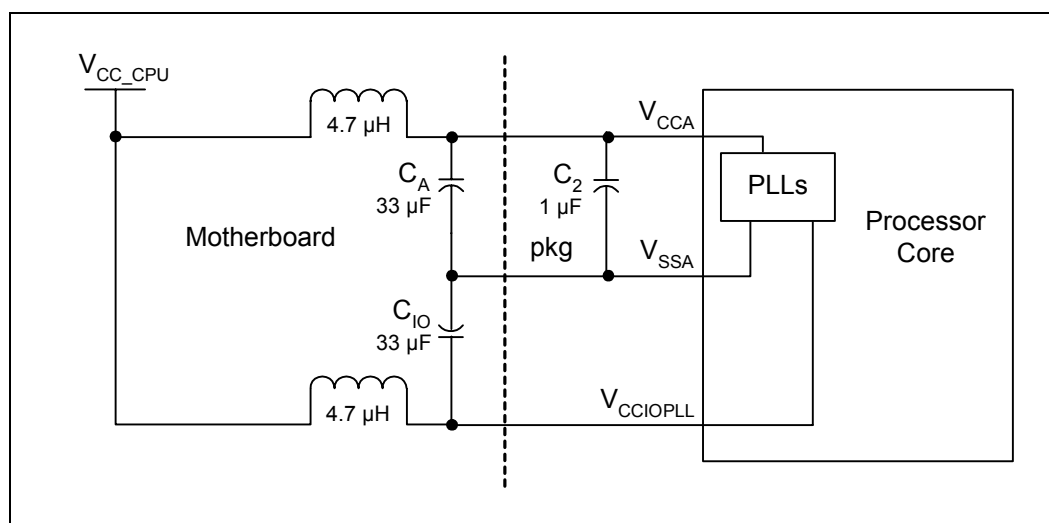
Figure 5-8. Routing Illustration for PWRGOOD



5.4.1.5 Topology 3: VCCIOPLL, VCCA and VSSA

VCCIOPLL and VCCA are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Keep these signals away from noisy or high-frequency signals. Keep their traces as short as possible. Follow the recommendations in [Figure 5-9](#) for layout guidelines. VSSA should not be connected directly to ground on the system board. Further details can be found in [Section 12.6](#)

Figure 5-9. Routing Illustration for VCCIOPLL, VCCA and VSSA



5.4.1.6 Topology 4: BR0# and RESET#

Since the processor does not have on-die termination on the BR0# and RESET# signals, it is necessary to terminate using discrete components on the system board. Connect the signals between the components as shown in Figure 5-10. The E7205 chipset has on-die termination and thus it is necessary to terminate only at the processor end. The value of R_T should be $51\Omega \pm 5\%$ for RESET#. The value of R_T should be $150\Omega - 220\Omega \pm 5\%$ for BR0#.

Figure 5-10. Routing Illustration for BR0# and RESET#

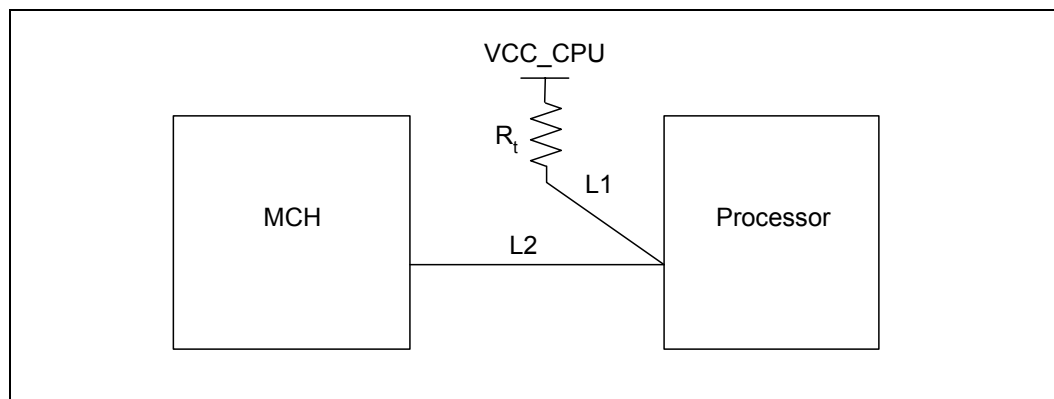


Table 5-9. BR0# and RESET# Lengths

Signal	R_T	L1	L2
RESET#	51Ω	$\leq 1'' - 2''$	$2.5'' - 10''$
BR0#	$150 - 220\Omega$	$\leq 1'' - 2''$	$2.5'' - 10''$

5.4.1.7 Topology 5: XCOMP/YCOMP Signals

Terminate the XCOMP/YCOMP pins to ground through two resistors. Refer to the latest schematics for the resistor values. Do not wire the COMP pins together; connect each pin to its own termination resistor.

5.4.1.8 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the Processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses and address buses etc. are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

5.4.1.9 Topology 7: TESTHI and RESERVED Pins

TESTHI[11:8] and TESTHI1 must be connected to VCC_CPU via a pull-up resistor. TESTHI[5:2], TESTHI0, and TESTHI12 must be connected to VCC_CPU via a pull-up resistor or be tied directly to VCC_CPU. Ideally, each TESTHI pin should be pulled up with a resistor value that matches the impedance of the system bus interface. If a value matching the system bus interface is not possible, each signal must use a pull-up resistor with a value between 40 Ω and 60 Ω .

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be tied directly to VCC_CPU, or connected individually to VCC_CPU using pull-up resistors with values between 1 k Ω and 10 k Ω . Tying ITPCLKOUT[1:0] directly to VCC_CPU or sharing a pull-up resistor to VCC_CPU, will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

5.4.1.10 Topology 8: VCCVID Regulator Recommendations

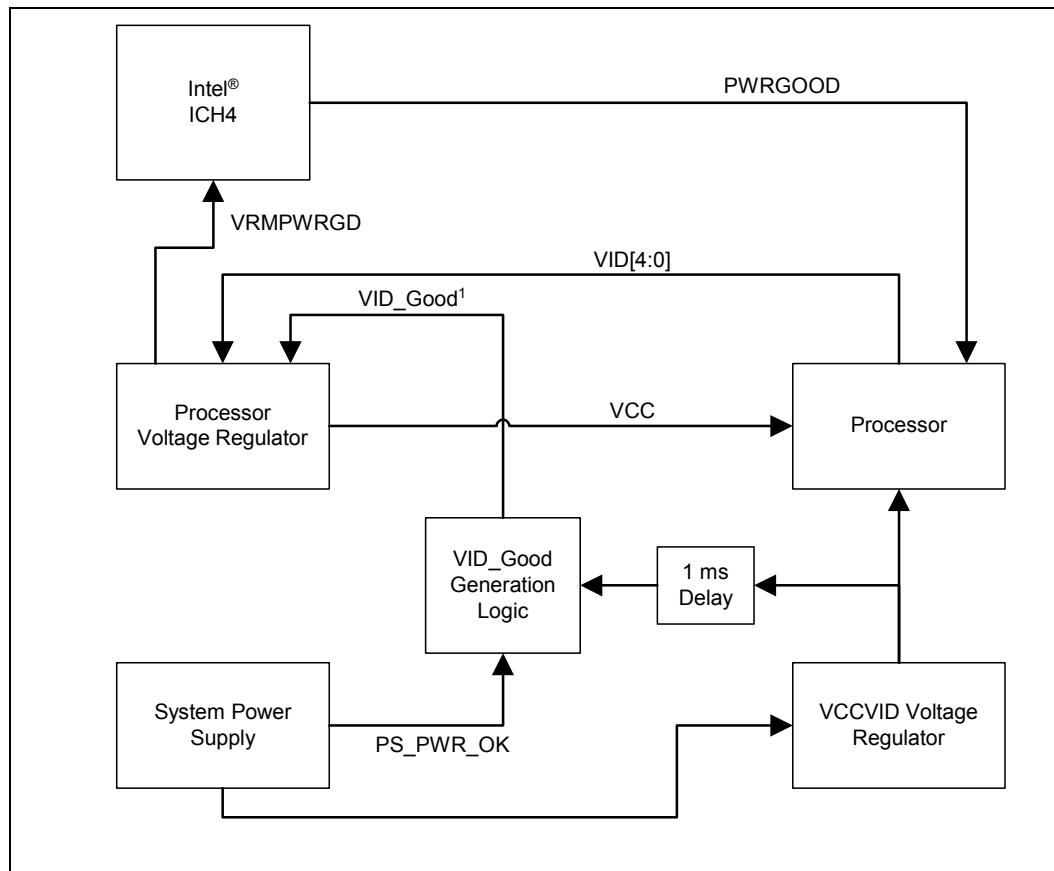
- The output of the voltage regulator used to generate VCCVID should be no more than 1.5 inches away from pin AF4 of the processor.
- The trace connecting the voltage regulator output to pin AF4 should be as wide as practical, but not less than 0.025 inches.
- The trace connecting the voltage regulator output to pin AF4 should have both a 0.1 μ F and 1.0 μ F capacitor for decoupling. The 1.0 μ F capacitor should be located as close as possible to the output of the voltage regulator. The 0.1 μ F capacitor should be located as close as possible to pin AF4 on the processor.

If an integrated voltage regulator such as the MIC5248 is used, the voltage input (pin 1) should be connected to the system boards VCC or 3.3 V rails through a zero ohm resistor. The input of the voltage regulator should also be decoupled with a 0.1 μ F capacitor at the pin. The trace connecting the voltage regulator input to the zero resistor should be equal to or greater than the voltage regulator output trace connected to the processor (i.e. if the connection to the processor is 0.025 inches then the trace width to the input of the voltage regulator should be 0.025 inches or greater). The voltage regulator power good signal (pin 4) should be connected to the voltage regulator output (pin 5) through a 10 k Ω resistor.

5.4.1.11 Topology 9: Processor Voltage Regulator Sequencing Requirements

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process requires a 1.3 V supply to the VCCVID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 5-11 shows a block diagram of a power sequencing implementation. Figure 5-12 and Figure 5-13 illustrate timing diagrams of the power sequencing requirements.

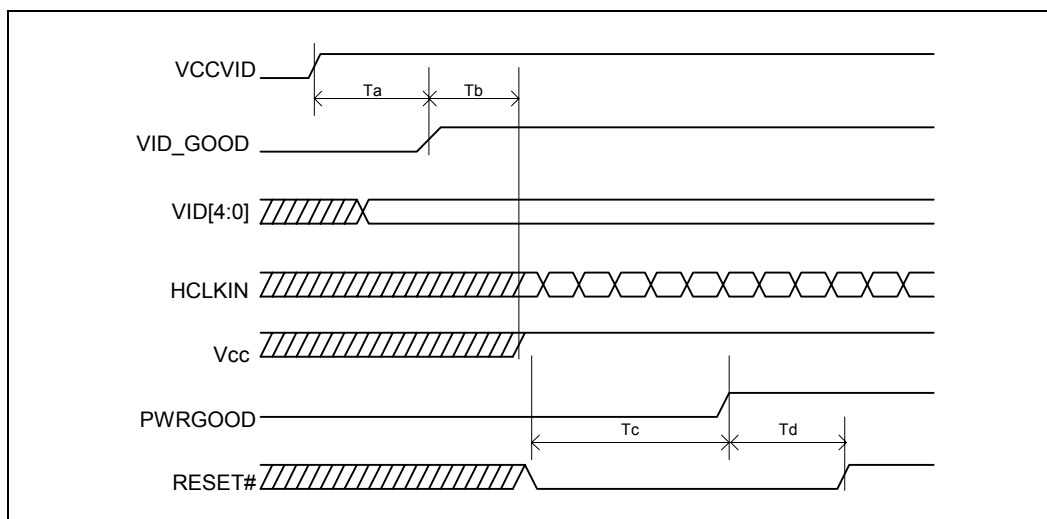
Figure 5-11. Power Sequencing Block Diagram



NOTES:

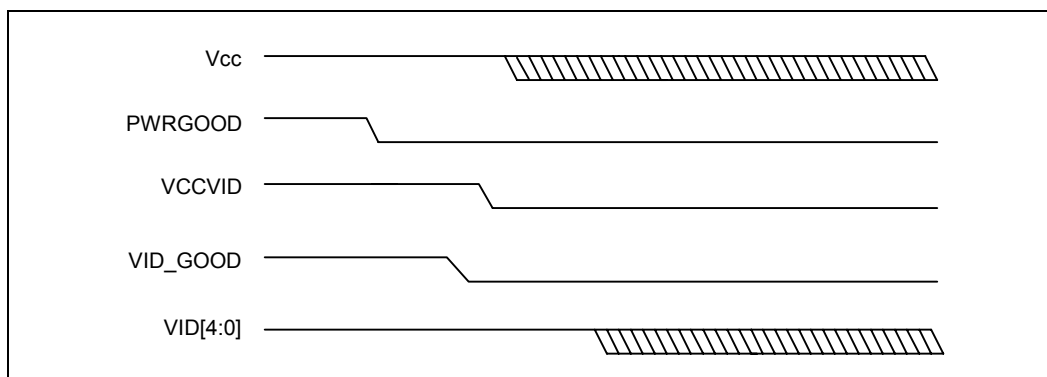
1. VID_Good connected to voltage regulator controller output enable.

Figure 5-12. Power-on Sequence Timing Diagram

**NOTES:**

1. $T_a = 1$ ms minimum (VCCVID > 1V to VID_GOOD high)
2. $T_b = 50$ ms maximum (VID_GOOD to VCC valid maximum time)
3. $T_c = T_{37}$ (PWRGOOD inactive pulse width) = 10 BCLKs min
4. $T_d = T_{36}$ (PWRGOOD to RESET# de-assertion time) = 1 ms (min), 10 ms (max)
5. VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regulator control silicon.

Figure 5-13. Power-off Sequence Timing Diagram

**NOTES:**

1. This timing diagram is not intended to show specific times. Instead a general ordering of events with respect to time should be observed.
2. When VCCVID is less than 1 V, VID_GOOD must be low.
3. VCC must be disabled before VID[4:0] becomes invalid.
4. VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regulator control silicon.

DDR System Memory Design Guidelines

6

This chapter contains information and details for designing an E7205 chipset-based platform with DDR PC2100. The chapter provides information on the DDR reference stack-up, topologies, and DDR layout, and routing guidelines for each system memory interface signal group that is described. This chapter also provides system memory bypass capacitor guidelines and DDR power deliver requirements. Together, these guidelines provide for a robust DDR solution for an E7205 chipset-based design.

As system memory transfer rates increase, careful attention must be given to all of the E7205 chipset guidelines to provide system robustness for DDR PC2100.

As stated earlier, the MCH is a dual channel memory interface. The pinout for the two channels has been optimized for a motherboard design with interleaved DIMMs. The DIMM closest to the MCH is DIMM0 on channel A, the next DIMM is DIMM0 on Channel B. The DIMMs continue to alternate between Channel A and B to the termination resistors.

The Double Data Rate (DDR) SDRAM system memory interface supports unbuffered memory only. The system memory interface can be divided into six signal groups: Data, Address/Command, Control, Feedback, Clocks and DC bias signals. [Table 6-1](#) summarizes the signal groupings. Refer to the *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet* for more information about these signals.

The E7205 chipset supports Error Checking and Correction (ECC).

Table 6-1. Intel® E7205 Chipset DDR Signal Groups

Group	Signal Name
Control	CKE_x[3:0]
	CS_x[3:0]#
Clocks	CMDCLK_x[7:0]
	CMDCLK_x[7:0]#
Data	DQ_x[63:0]
	DQS_x[17:0]
	CB_x[7:0]
Address / Command	MA_x[12:0]
	BA_x[1:0]
	RAS_x#
	CAS_x#
	WE_x#
DC Biasing	RCVENOUT_x#
DC Bias	DRCOMP_H
	DRCOMP_V
	ODTCOMP
	DRCOMPVREF_H
	DRCOMPVREF_V
	DDR_STRAP
	DVREF_A / DVREF_B

6.1 DDR-SDRAM Stack-Up and Referencing Guidelines

The E7205 chipset platform designs using the DDR-SDRAM memory sub-system require continuous ground referencing for all DDR signals. Based on the six-layer stack-up shown below, the DDR channel is completely ground referenced. Although the DDR bus is technically referencing both power and ground on layer 4, it is much more tightly coupled to the ground plane because it is closer to the ground plane. Attention still must be paid to ensure that DDR signals do not cross power plane splits because a small percentage of the return current travels through the power planes.

All DDR signals must be ground referenced to provide an optimal current return path. To do this, the ground plane must be solid and continuous from the MCH DDR signal pins to beyond the VTT termination capacitors at the end of the channel.

Figure 6-1. Board Stack-Up

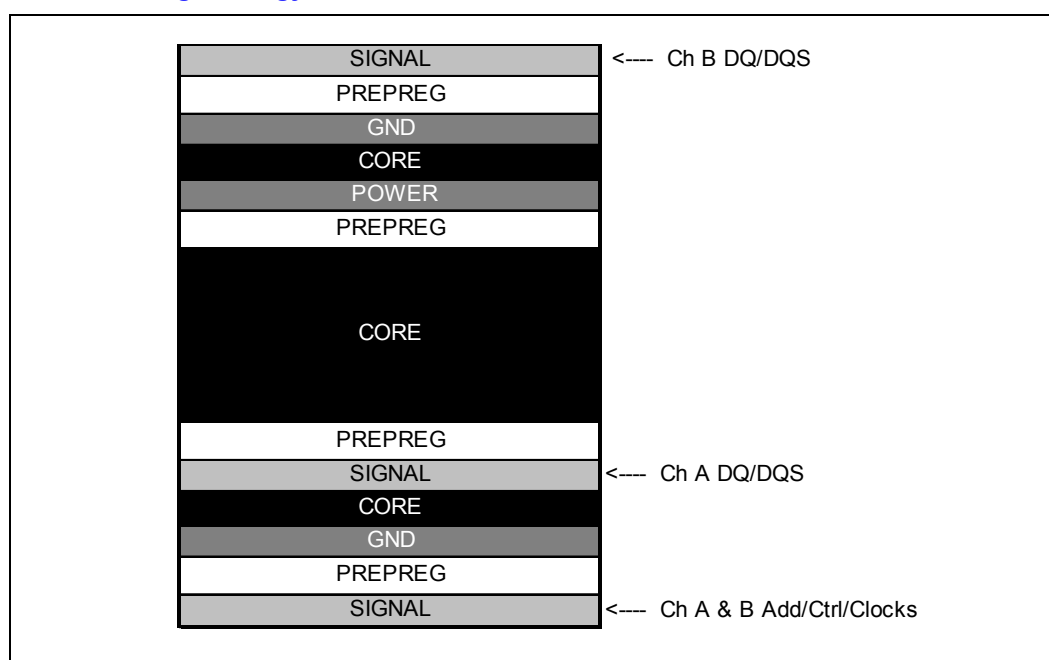
		Layer Thickness	Copper Weight
Top	SIGNAL	2.1	0.5 oz plus plating
	PREPREG	4.0	
Layer 2	GND	1.2	1 oz.
	CORE	4.3	
Layer 3	POWER	1.2	1 oz.
	PREPREG	6.5	
	CORE	23.0	
	PREPREG	6.5	
Layer 4	SIGNAL	1.2	1 oz.
	CORE	4.3	
Layer 5	GND	1.2	1 oz.
	PREPREG	4.0	
Bottom	SIGNAL	2.1	0.5 oz plus plating
Panel Thickness (mils) =		61.6	Assumes finished thickness on uStrip Layers

6.2 Unbuffered DDR System Memory Topology and Layout Design Guidelines

This section contains information and details on the DDR topologies, layout and routing guidelines. The guidelines are provided for each corresponding signal group: Data, Address/Command, Control, Feedback, Clock and DC biasing.

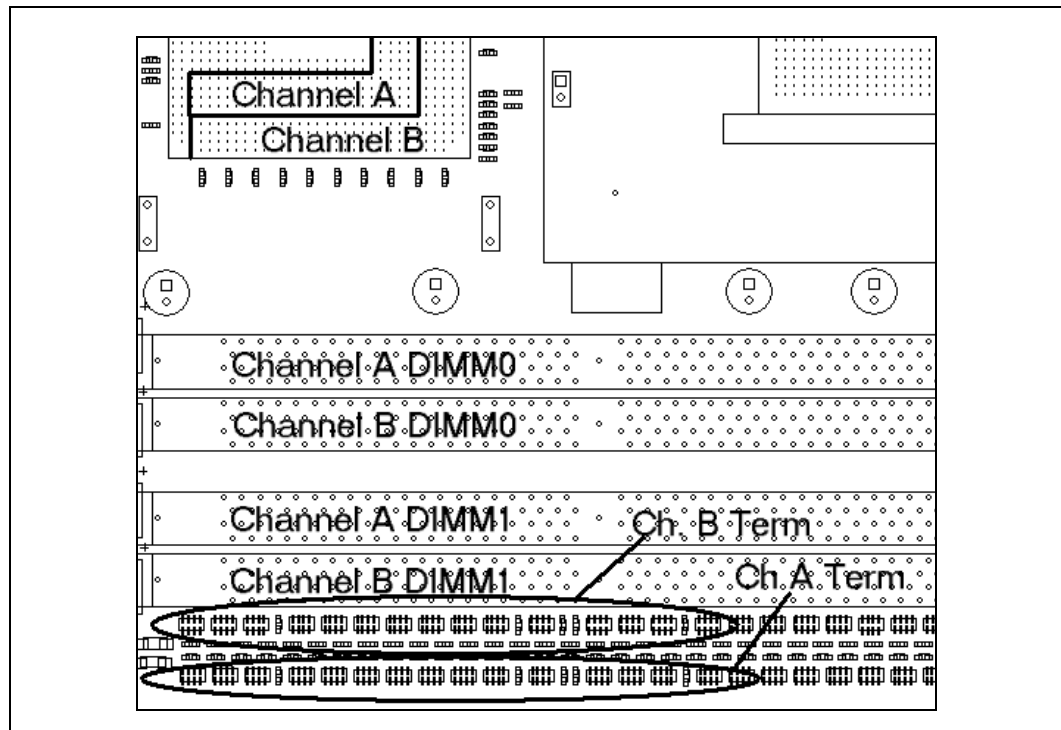
The MCH has two channels of DDR memory. All signals can break out of the MCH and route entirely referenced to ground. The general routing strategy in a 6-layer board is to route all the data and strobcs for Channel B (closest to edge of MCH package) on the top layer. The Channel A data and strobcs can be routed entirely on the layer 4. The address, control and clock signals for both channels can be routed entirely on the bottom layer. With this strategy, the whole interface will be ground referenced. The specific details of those individual topologies will be shown in the following sections.

Figure 6-2. DDR Routing Strategy



Because of the height-restricted areas of the ATX chassis, it is best to place the DIMMs as close to the back of the chassis as possible. With the E7205 chipset platform having interleaved DIMMs, placing the termination resistors immediately after the last DIMM in Channel A, physically the third DIMM from the MCH was not ideal. Instead, the termination resistors for both channels were placed beyond the last DIMM. The result of this is that lengths to termination resistors on Channel A grow larger than previous DDR designs, especially for chip selects and clock enable signals. The additional advantage of this is that Channel B data and strobcs can be routed on the top layer with no layer transitioning. The Channel A data and strobcs transition to layer 4 at the MCH and can route to the DIMMs and return to the top layer to terminate at the resistor pads. The same is true for the clocks, control and address signals which are routed on the bottom layer.

Figure 6-3. DDR DIMM and Termination Strategy



The following signaling group sections are intentionally ordered in the same fashion that Intel recommends approaching the length matching criteria. The CKE and CS# signals should be routed first and made as short as possible. From those lengths, the required command clock group lengths are determined which will drive the required lengths for the data/strobe groups and address/control groups, respectively.

6.2.1 Control Signals — CKE_x[3:0], CS_x[3:0]#

The MCH control signals are source-clocked signals that include 4 clock enable (CKE) and 4 chip selects (CS#) signals. These control signals are clocked into the DIMMs using the positive edge of the differential clock signals. The Intel MCH drives the control signals and clocks signals together, with the clocks centered in the valid control window. Only one chip select (CS#) and one clock enable (CKE) signal is needed for each DDR-SDRAM physical DIMM device row.

Two chip selects and two clock enables are routed to each DIMM (one for each side) to support double-sided DDR DIMMs. [Table 6-2](#) below summarizes the CKE/CS# to DIMM pin mapping.

Table 6-2. Control Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CS_x0#	DIMM0	157
CS_x1#	DIMM0	158
CS_x2#	DIMM1	157
CS_x3#	DIMM1	158
CKE_x0	DIMM0	21
CKE_x1	DIMM0	111
CKE_x2	DIMM1	21
CKE_x3	DIMM1	111

Resistor packs are acceptable for the parallel control termination resistors (R_{TT}), but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, address/command signals.

[Table 6-3](#) and [Figure 6-4](#) through [Figure 6-6](#) depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals for the first and second DIMM.

Figure 6-4. DIMM-0 Control Signal Routing Topology (CS_x[1:0]#, CKE_x[1:0])

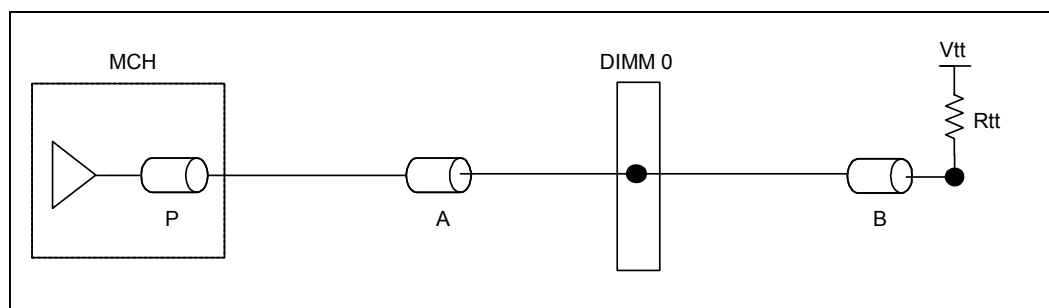


Figure 6-5. DIMM-1 Control Signal Routing Topology (CS_x[3:2]#, CKE_x[3:2])

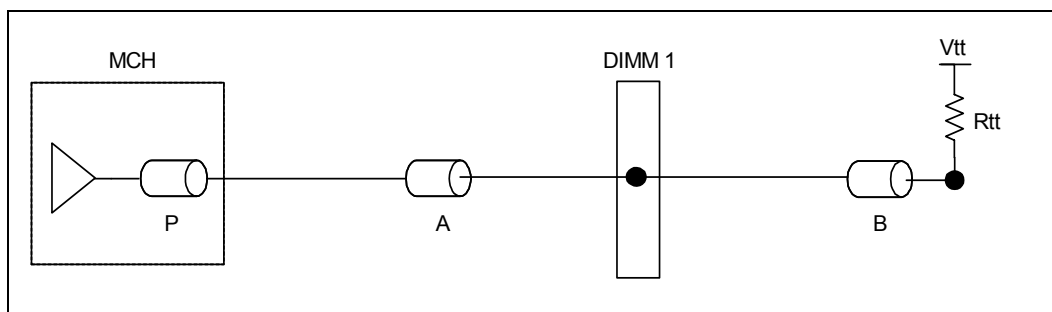
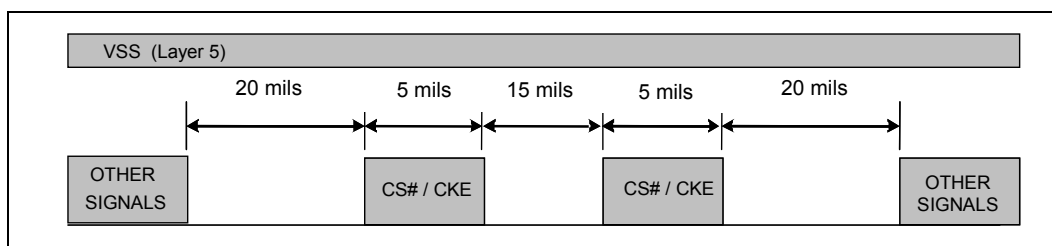


Table 6-3. Control Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CS _x [3:0]#, CKE _x [3:0]
Topology	Point-to-point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	A, B = $60 \Omega \pm 10\%$
Nominal Trace Width	A, B = 5 mils
Nominal Trace Spacing	MCH to first DIMM = 15 mils
Group Spacing	20 mils minimum spacing from non-DDR related signals.
Trace Length A (CS _x [1:0]#/CKE _x [1:0]) – MCH Signal Ball to DIMM Pins on First DIMM	CS#: 1.5" – 5.5" CKE: 1.5" – 5.5"
Trace Length A (CS _x [3:2]#/CKE _x [3:2]) – MCH Signal Ball to DIMM Pins on Second DIMM	CS#: 1.5" – 5.5" CKE: 1.5" – 5.5"
Trace Length B (CS _x [1:0]#/CKE _x [1:0]) – DIMM pins on first DIMM to R _{TT} Pad	CS#: 0.1" – 2.5" CKE: 0.1" – 2.5"
Trace Length B (CS _x [3:2]#/CKE _x [3:2]) – DIMM pins on Second DIMM to R _{TT} Pad	CS#: 0.1" – 2.5" CKE: 0.1" – 2.5"
Termination Resistor (R _{TT})	$56 \Omega \pm 5\%$
MCH Breakout Guidelines	5 mil width using maximum spacing until broken out beyond the MCH package.
Length Tuning Method	CS _x [3:0]#/CKE _x [3:0] do not have length matching requirements. Keep as short as possible because the longest CS# or CKE length drives the minimum CMDCLK length. See the following section for details.

Figure 6-6. Control Signal Trace Width/Spacing Routing on Lead-in Length



6.2.1.1 Control Group Signal Length Matching Requirements

The CS# and CKE signals do not require length matching but must be routed as short as possible. As an example, CS_x[1:0]# and CKE_x[1:0] will be routed to the first DIMM in either Channel A or Channel B. After routing those four signals, the longest net, which includes the MCH internal package length, will drive the minimum length for the clocks to the first DIMM in the channel, CMDCLK_x[0,4,6] and CMDCLK_x[0,4,6]#. It's important to include the internal lengths in calculating the longest net because the longest net on the board may not be the longest net from MCH die pad to DIMM pin.

6.2.2 Clock Signals — CMDCLK_x[7:0], CMDCLK_x[7:0]#

The MCH clock signals include 8 differential clock pairs CMDCLK_x[7:0] and CMDCLK_x[7:0]#. In an unbuffered configuration, CMDCLK_x[3:2] and CMDCLK_x[3:2]# are left floating because only six pairs are needed for a 2-DIMM per channel configuration. The MCH generates and drives these differential clock signals required by the DDR interface; therefore no external clock driver is required for the DDR interface. Three differential clock pairs are routed to each DIMM connector. [Table 6-4](#) summarizes the clock signal mapping.

Table 6-4. Clock Signal Mapping

Signal	Routed to
CMDCLK_x[0,4,6], CMDCLK_x[0,4,6]#	DIMM0
CMDCLK_x[1,5,7], CMDCLK_x[1,5,7]#	DIMM1
CMDCLK_x[2,3],CMDCLK_x[2,3]#	No Connect

The differential clock pairs must be routed differentially from the MCH to their associated DIMM pins, and must maintain the correct isolation spacing from other signals. When the signals serpentine, maintain a minimum of 20-mil spacing. The differential clock pair must maintain correct spacing to remain differential.

Table 6-5 is provided to help the routing of the clock signals. The table summarizes a typical clock signal to DIMM pin mapping.

Table 6-5. Clock Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CMDCLK_x0	DIMM0	137
CMDCLK_x0#	DIMM0	138
CMDCLK_x4	DIMM0	16
CMDCLK_x4#	DIMM0	17
CMDCLK_x6	DIMM0	76
CMDCLK_x6#	DIMM0	75
CMDCLK_x1	DIMM1	137
CMDCLK_x1#	DIMM1	138
CMDCLK_x5	DIMM1	16
CMDCLK_x5#	DIMM1	17
CMDCLK_x7	DIMM1	76
CMDCLK_x7#	DIMM1	75

The CS# and CKE lengths drive the minimum length requirements for the command clocks. The rest of the DDR system memory signals are tuned to CMDCLK/CMDCLK#. The individual group signal length matching requirements are detailed in their corresponding section for each system memory group. CMDCLK/CMDCLK# must be length-matched to each other.

No external termination resistors are needed for the clock signals. Table 6-6 and Figure 6-7 through Figure 6-9 show the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 6-7. DDR Clock Routing Topology (CMDCLK_x[0,4,6]/CMDCLK_x[0,4,6]#)

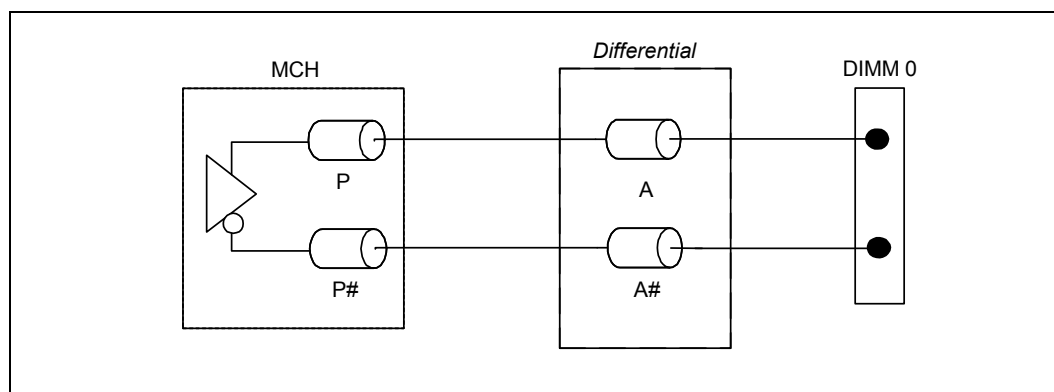


Figure 6-8. DDR Clock Routing Topology (CMDCLK_x[1,5,7]/CMDCLK_x[1,5,7]#)

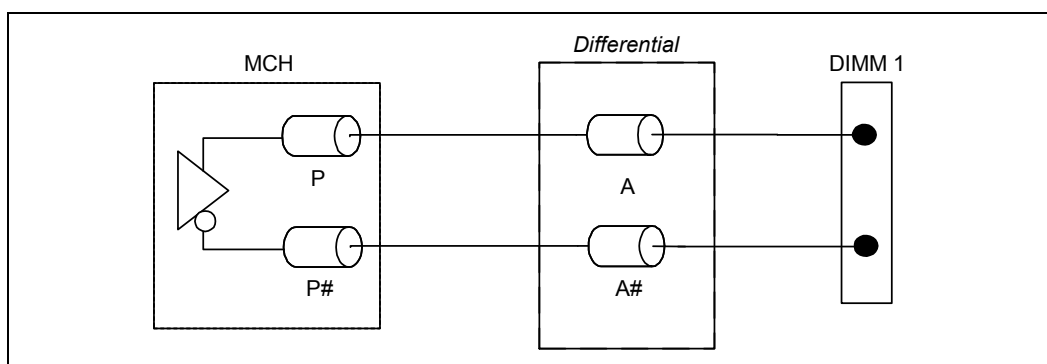
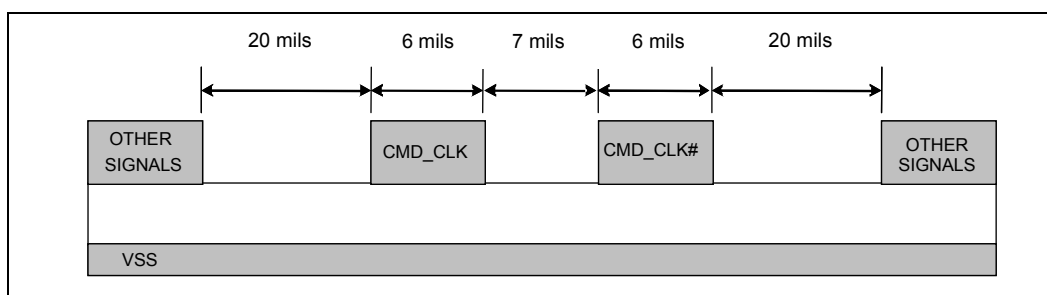


Table 6-6. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CMDCLK_x[7:4,1:0]/CMDCLK_x[7:4,1:0]#
Topology	Point-to-point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	Differential = $84 \Omega \pm 10\%$
Nominal Trace Width	6 mils
Nominal Differential Trace Spacing	7 mils
Group Spacing	20 mils minimum spacing from another DDR signal group. 20 mils minimum spacing from non-DDR related signals.
Serpentine Spacing	20 mils minimum
Trace Length A (CMDCLK_x[0,4,6]) – MCH Signal Ball to pin of first DIMM	Min = 3.5" Max = 9.0"
Trace Length A (CMDCLK_x[1,5,7]) – MCH Signal Ball to pin of Second DIMM	Min = 3.5" Max = 9.0"
MCH Breakout Guidelines	5-mil width with 5-mil differential spacing until broken out of package.
Length Matching	Exact length matching from MCH internal die pad to DIMM connector pin is required for CMDCLKs and their complements. In addition, CMDCLKs must length match the other command clocks connecting to the same DIMM, i.e., CMDCLK_x0 must match CMDCLK_x4 and CMDCLK_x6 which all route to the first DIMM.

Figure 6-9. Clock Signal Trace Width/Spacing Routing Cross Section



6.2.2.1 Clock Group Signal Length Matching Requirements

The MCH provides three differential clock pair signals for each DIMM. A differential clock pair consists of a CMDCLK signal and its complement signal CMDCLK#. In the previous section, it was advised that the CS# and CKE signals be routed as short as possible. Including the MCH internal package lengths in the comparison, the longest CS# or CKE is determined. From this net, the minimum length of the command clocks is determined. The longest net within CS_x[1:0]# and CKE_x[1:0] will determine the minimum length of CMDCLK_x[0,4,6]. The longest net within CS_x[3:2]# and CKE_x[3:2] will determine the minimum length of CMDCLK_x[1,5,7].

If the longest CKE has a lead-in length between:

	1.5 - 2.5"	then the minimum CMDCLK length \geq CKE + 2.0"
or	2.5 - 3.5"	then the minimum CMDCLK length \geq CKE + 2.5"
or	3.5 - 4.0"	then the minimum CMDCLK length \geq CKE + 3.0"
or	4.0 - 5.5"	then the minimum CMDCLK length \geq CKE + 3.5"

If the longest CS# has a lead-in length between:

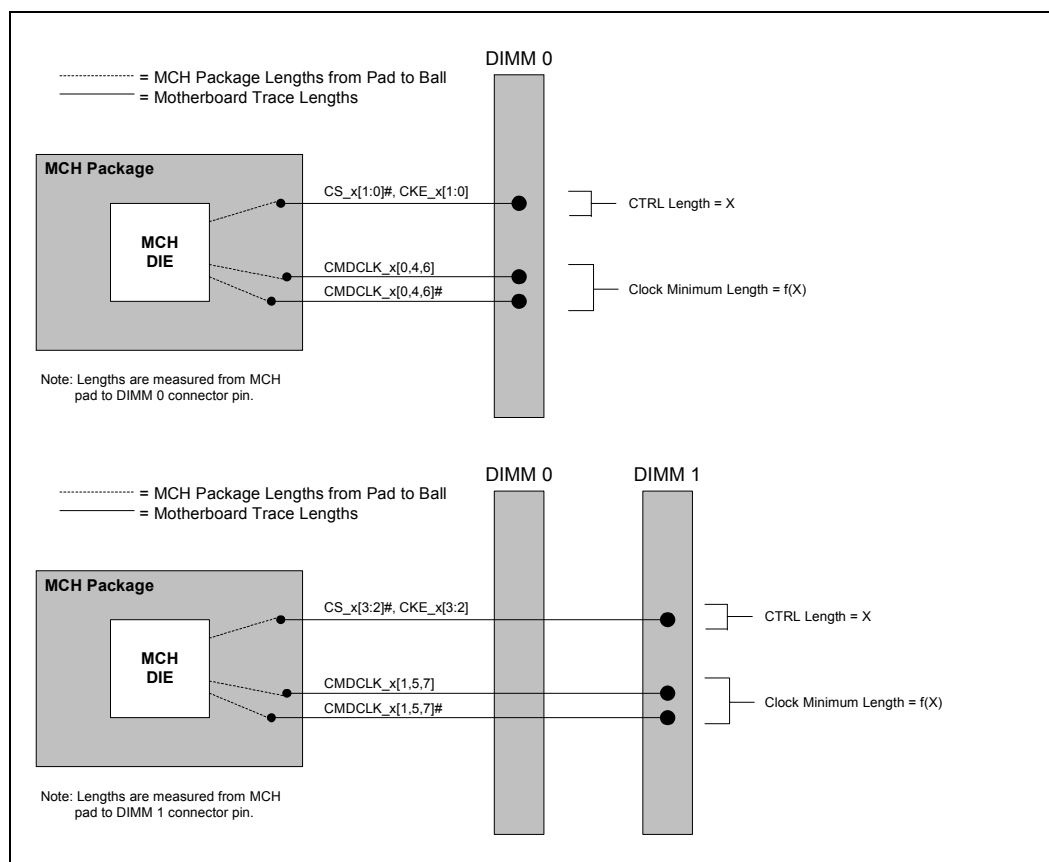
	1.5 - 2.5"	then the minimum CMDCLK length \geq CS# + 1.0"
or	2.5 - 3.0"	then the minimum CMDCLK length \geq CS# + 1.5"
or	3.0 - 3.5"	then the minimum CMDCLK length \geq CS# + 2.0"
or	3.5 - 4.5"	then the minimum CMDCLK length \geq CS# + 2.5"
or	4.5 - 5.5"	then the minimum CMDCLK length \geq CS# + 3.0"

It is important to compare the CS# and CKE lengths after the previous equations have been applied to determine the minimum command clock length. For instance, a CS# length of 2 inches and a CKE length of 1.9 inches would suggest the CS# signal would create the longest minimum command clock length requirement. After applying the equations, the CS# length is adjusted to 3 inches (2" + 1") and the CKE length is adjusted to 3.9 inches (1.9" + 2.0"). Therefore, the longest adjusted net is actually the CKE signal and it will determine the minimum command clock length.

From the above equations, it is clear why the CS# and CKE signals must be as short as possible. The maximum control signal length drives the command clocks to be longer. This requires the data and strobe signals to increase in length as well.

Figure 6-10 shows the length matching requirements between the control and the clock signals.

Figure 6-10. Control Signal to CMDCLK Trace Length Matching Requirements



CMDCLK and its complement CMDCLK# within each differential clock pair requires exact length matching from MCH pad to the pins of the DIMM connector.

The length of the CMDCLK and its complement to first and second DIMM include the MCH package length + the motherboard trace length. The internal package trace lengths is provided in the *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet*.

In addition, clock length matching is required between clock pairs associated to the same DIMM. The differential clock pairs for the first DIMM connector, CMDCLK_x[0,4,6]/CMDCLK_x[0,4,6]#, require exact matching of the trace lengths from MCH internal pad to the pins of the first DIMM connector. The differential clock pairs for the second DIMM connector, CMDCLK_x[1,5,7]/CMDCLK_x[1,5,7]#, require exact matching of the trace lengths from MCH internal pad to the pins of the second DIMM connector.

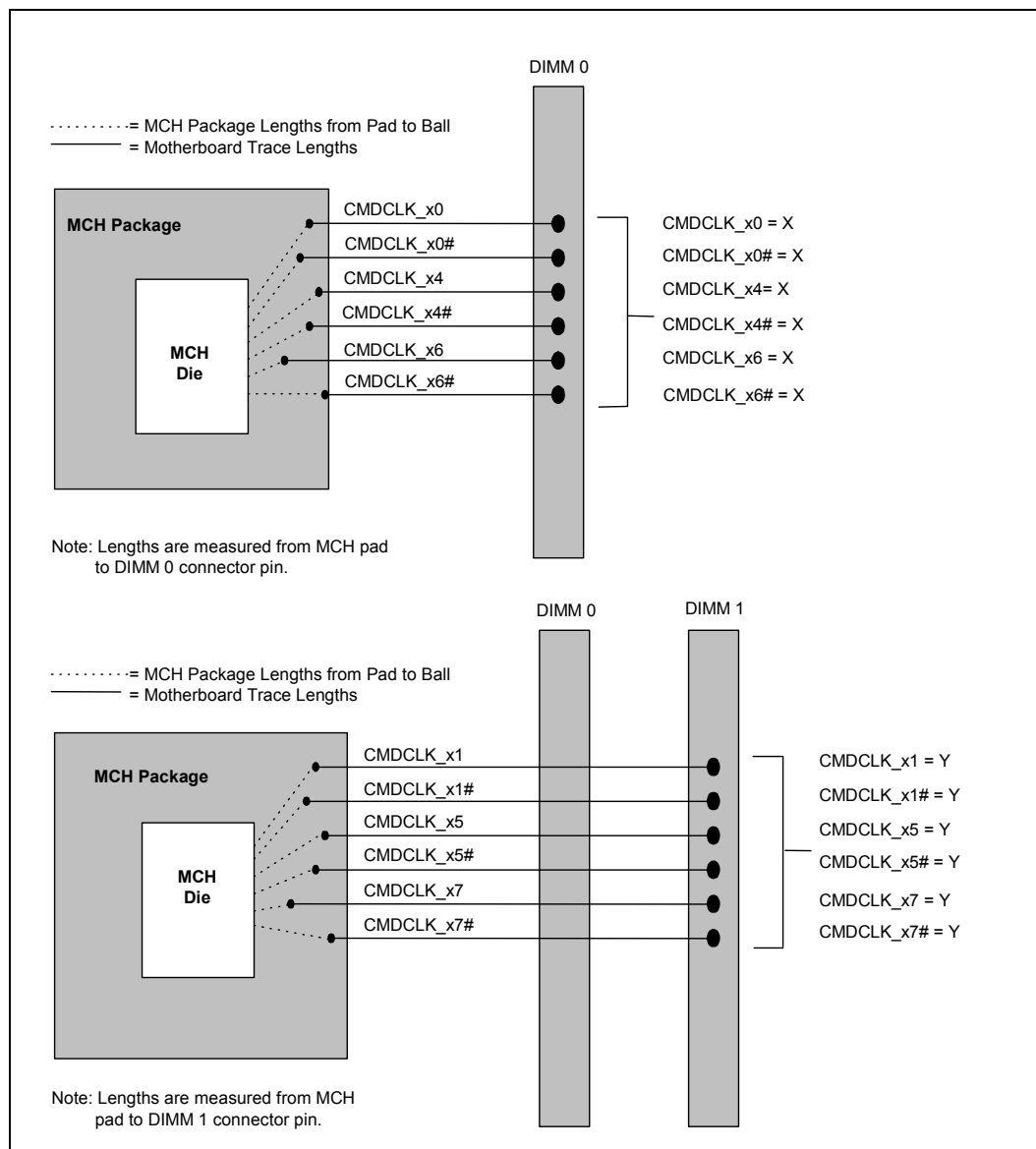
$$\begin{aligned} \text{CMDCLK_x0} &= \text{CMDCLK_x0\#} = \text{CMDCLK_x4} = \text{CMDCLK_x4\#} = \text{CMDCLK_x6} \\ &= \text{CMDCLK_x6\#} \end{aligned}$$

and

$$\begin{aligned} \text{CMDCLK_x1} &= \text{CMDCLK_x1\#} = \text{CMDCLK_x5} = \text{CMDCLK_x5\#} = \text{CMDCLK_x7} \\ &= \text{CMDCLK_x7\#} \end{aligned}$$

Note that the differential clocks must also be tuned with the data strobes, address/command, and control signals. Figure 6-11 shows the length matching requirements for the differential clock signals.

Figure 6-11. CMDCLK to CMDCLK# Trace Length Matching Requirements



6.2.3 Data Signals — DQ_x[63:0], DQS_x[17:0], CB_x[7:0]

The MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits, and 9 data strobe signals. DQS_x[17:9] are needed only for x4 devices that are unique to registered memory. The signals DQS_x[17:9] can be tied directly to ground at the DIMMs.

Table 6-7 summarizes the DQ/CB to DQS mapping.

Table 6-7. Signals and Associated Strobe

Signal	Associated Strobe
DQ_x[7:0]	DQS_x0
DQ_x[15:8]	DQS_x1
DQ_x[23:16]	DQS_x2
DQ_x[31:24]	DQS_x3
DQ_x[39:32]	DQS_x4
DQ_x[47:40]	DQS_x5
DQ_x[55:48]	DQS_x6
DQ_x[63:56]	DQS_x7
CB_x[7:0]	DQS_x8

It is important to note that the DQ and CB signals must be length matched only to their associated DQS in board etch length—the lengths do not have to account for package compensation. The DQSs and DQ/CBs must match in length only from the MCH ball to DIMM pin. However, the strobe signals (DQS) do have to package compensate when determining their minimum length relative to the command clocks. The following sections provide more information on the length tuning method.

Resistor packs are acceptable for the parallel data and data strobe termination resistors (R_{TT}), but data and strobe signals should not be routed to the same resistor pack (RPACK) used by address/command, or control signals.

Figure 6-12 and Table 6-8 describe the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Note: It is important to note that the data/strobe groups require a “mixed impedance” topology. The lead-in length from the MCH to the first DIMM is a lower impedance than the segment connecting the first DIMM to the second DIMM and continuing to the termination resistor.

The variables in the figure are:

- P = MCH package trace from silicon to the package ball
- A = Board trace from the ball of the MCH to the first DIMM pin
- B = Board trace from the first DIMM to the second DIMM pin
- C = Board trace from the second DIMM pin to the termination resistor pin

Figure 6-12. Data Signal Routing Topology

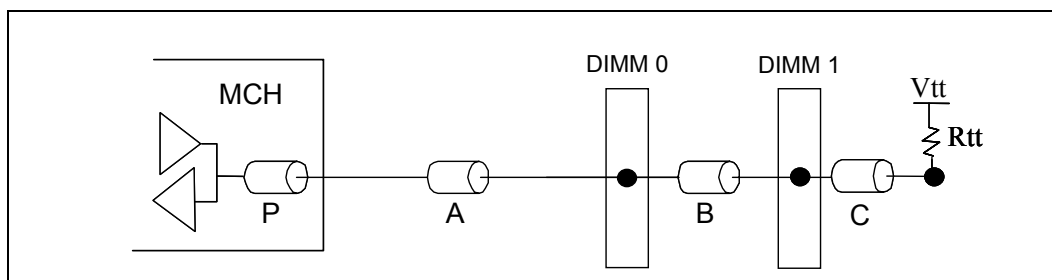


Table 6-8. Data Signal Group Routing Guidelines (Channel A and B)

Parameter	Routing Guidelines
Signal Group	DQ_x[63:0], CB_x[7:0], DQS_x[8:0]
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	A = 50 Ω , B, C = 60 $\Omega \pm 10\%$
Nominal Trace Width	A = 7 mils B, C = 5 mils
Nominal Trace Spacing	MCH to first DIMM = 10 mils data, 12 mils strobe Within DIMM Pin Field = 7 mils From DIMM to DIMM = 15 mils Second DIMM to Rtt = 15 mils
Group Spacing	20 mils minimum from non-DDR related signals.
Trace Length A – MCH Ball to First DIMM Pin	Min = 1.5" Max = 5.5"
Trace Length B – First DIMM Pin to Second DIMM Pin	Min = 1.1" Max = 1.2"
Trace Length C – DIMM Pin to termination resistor pad	Min = 0.1" Max = 1.5"
Termination Resistor (R_{TT})	39 $\Omega \pm 5\%$
MCH Breakout Guidelines	5 mil width with 5 mil spacing until beyond the package edge
Length Tuning Method	Length matching from the MCH internal die pad to the DIMM connector pin is required for DQ_x[63:0], CB_x[7:0] to DQS_x[8:0]. DQS_x[8:0] requires tuning to the DDR clock signals. See following sections for details.

6.2.3.1 Data Group Signal Length Matching Requirements

6.2.3.1.1 Strobe to Command Clock Length Matching Requirements

The tuning of strobes and differential clock signals must take into account the package lengths internal to the MCH package. Matching requires tuning from the MCH internal pad ball to the pins of the DIMM connector.

To Channel A first DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 3.0$ inches

To Channel B first DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 2.5$ inches

To Channel A second DIMM:

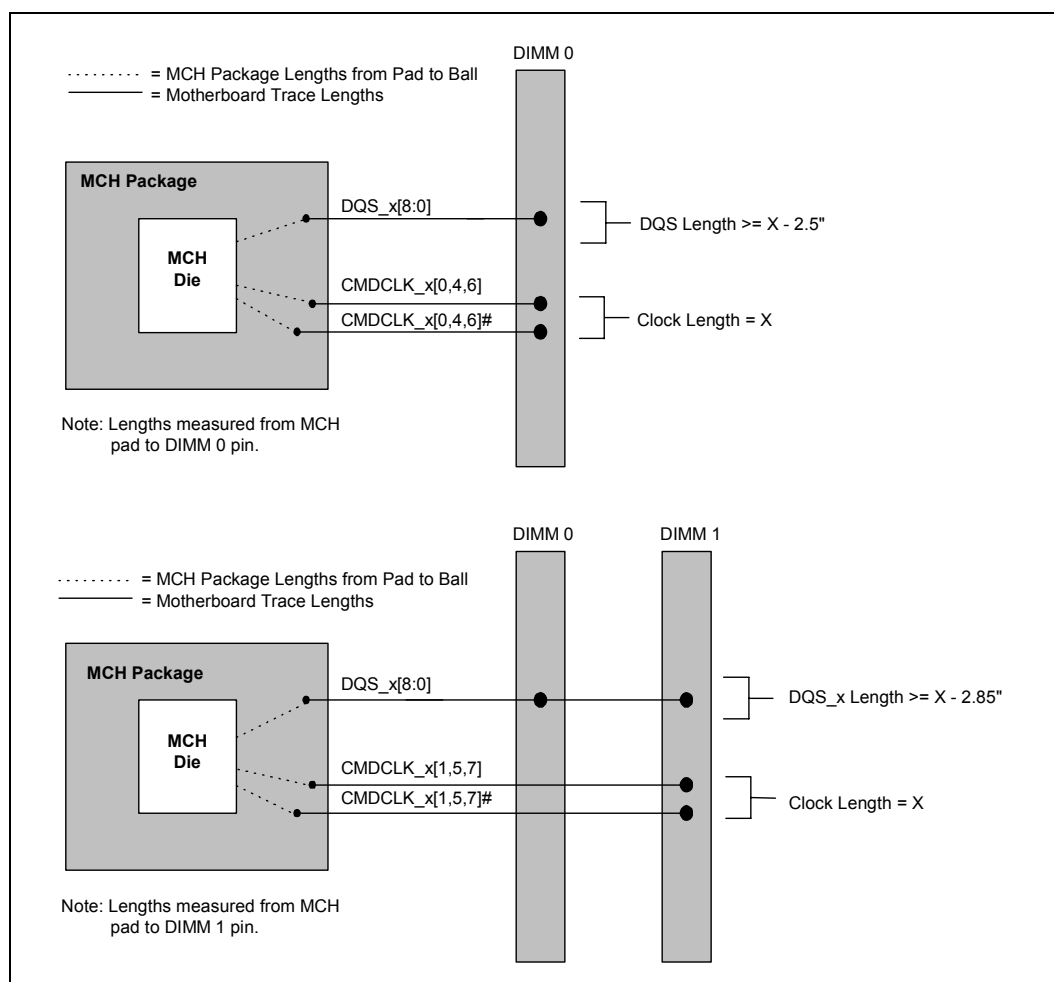
CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 3.3$ "

To Channel B second DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 2.8$ "

Length X and Y to first and second DIMM include the MCH package length + the motherboard trace length from the ball of the MCH to the DIMM. No length matching is required from the second DIMM to the parallel termination resistors. [Figure 6-13](#) shows the length matching requirements between the DQS and clock signals for Channel B only.

Figure 6-13. Channel B DQS to CMDCLK Trace Length Matching Requirements



6.2.3.1.2 Data to Strobe Length Matching Requirements

The tuning of the data strobes to the associated data and check bit signals does not require taking package length compensation into account. It is required that the strobes use package compensation when determining the required lengths relative to the command clocks as described in the previous section. However, length matching of the strobe to its associated data and check bits requires accounting only for the board etch. For instance, a command clock length to the first DIMM in Channel A equal to 8 inches requires that the strobe length to the first DIMM have a minimum length of 5 inches (8 inches – 3 inches) from die pad to DIMM. If the DQS_x0 happens to have 500 mils of internal package length, the board etch must be 4.5 inches. The eight signals, DQ_x[7:0], would then have to be routed to 4.5 inches, and do not require package compensation.

DQS Length = X,
 Associated DQ/CB Byte Group Length = Y,
 $(X - 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$

Length X and Y to first and second DIMM do not include the MCH package length—only the motherboard trace length. No length matching is required from the second DIMM to the parallel termination resistors.

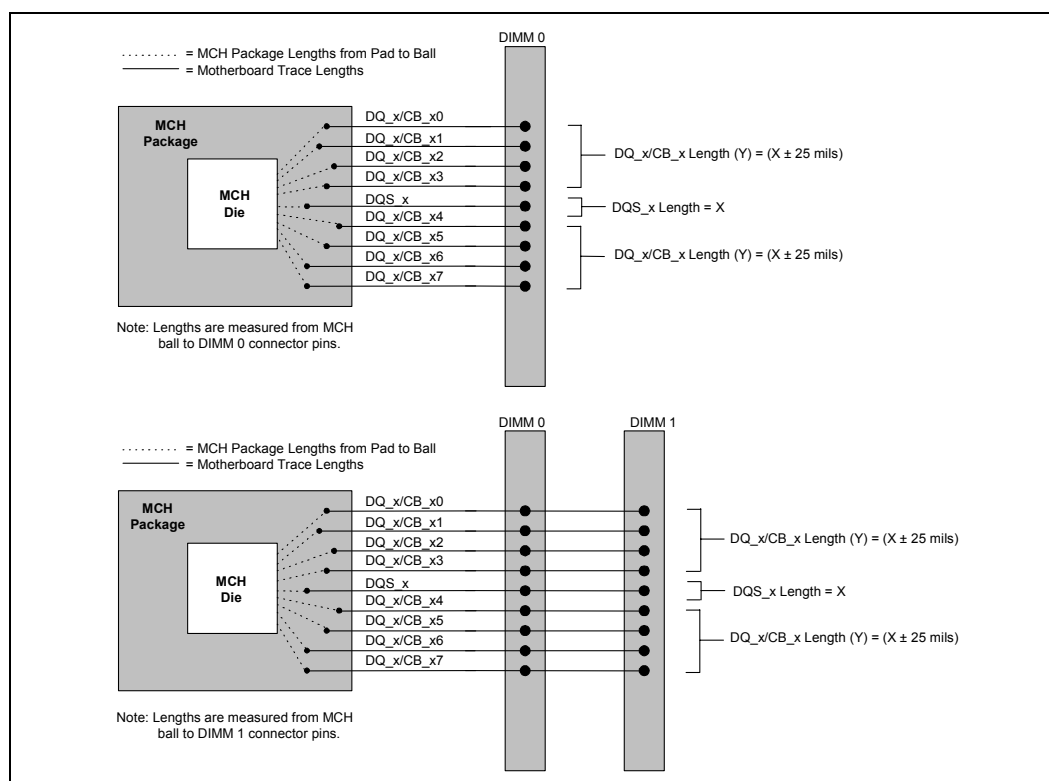
Table 6-9 and Figure 6-14 show the length matching requirements between the DQ, CB, and DQS signals.

Table 6-9. DQ/CB to DQS Length Matching Mapping

Signals	Length Mismatch	Relative to
DQ_x[7:0]	± 25 mils	DQS_x0
DQ_x[15:8]	± 25 mils	DQS_x1
DQ_x[23:16]	± 25 mils	DQS_x2
DQ_x[31:24]	± 25 mils	DQS_x3
DQ_x[39:32]	± 25 mils	DQS_x4
DQ_x[47:40]	± 25 mils	DQS_x5
DQ_x[55:48]	± 25 mils	DQS_x6
DQ_x[63:56]	± 25 mils	DQS_x7
CB_x[7:0]	± 25 mils	DQS_x8

It is important to note that the ± 25 mils tolerance must be divided between the segment from the MCH to the first DIMM, and the first DIMM to the second DIMM. For instance, a designer may use ± 15 mils of tolerance on the lead-in length to the first DIMM, and use ± 10 mils on the DIMM to DIMM segment. This ensures that the overall ± 25 mils requirement is met. If the ± 25 mils tolerance were used on each segment individually, a data signal's length could theoretically be out of specification by 25 mils at the second DIMM. The division of the tolerance is arbitrary, but allowing more lenience on the lead-in length is typically the easiest from a routing standpoint.

Figure 6-14. DQ/CB to DQS Length Matching



6.2.4 Address/Command Signals — MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#

The MCH address/command signals are source-clocked signals that include 13 system memory address (MA_x[12:0]), 2 bank address (BA), row address select (RAS_x#), column address select (CAS_x#), and write enable (WE_x#) signals. The address/command signals are clocked into the DIMMs using the positive edge of the differential clock signals. The MCH drives the address/command and clock signals together.

Resistor packs are acceptable for the series (R_s) and parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or control signals.

There is a required length relationship between the command clocks and the address/command signals, but it usually comes out naturally through normal routing without extra consideration. Details are explained in the following section.

Table 6-10 and Figure 6-15 and Figure 6-16 show the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 6-15. Address/Command Signal Routing Topology

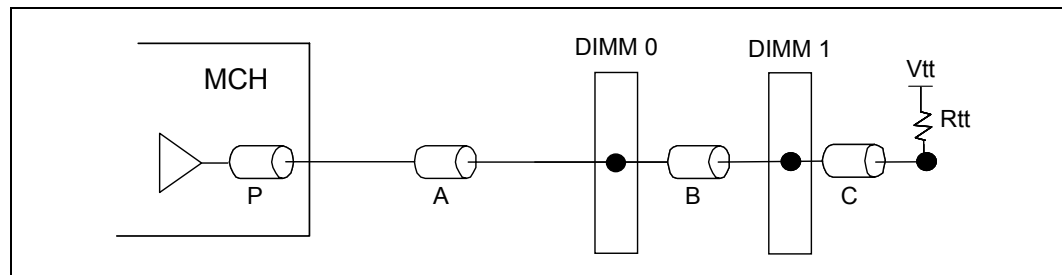
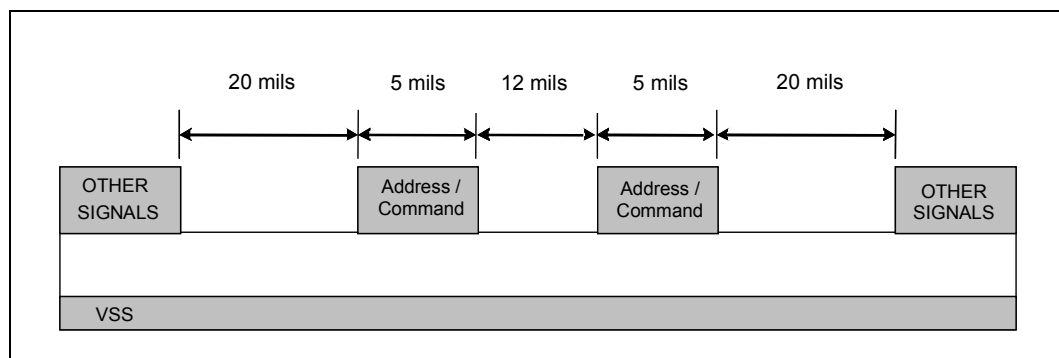


Table 6-10. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#
Topology	Daisy chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	A, B, C = $60 \Omega \pm 15\%$
Nominal Trace Width	A, B, C = 5 mils
Nominal Trace Spacing from MCH	MCH to first DIMM = 12 mils Within DIMM Pin Field = 7 mils From DIMM to DIMM = 12 mils Second DIMM to Rtt = 12 mils
Group Trace Spacing	20 mils spacing from non-DDR related signals.
Trace Length A – MCH Signal Ball to DIMM 1 pin	Min = 1.5" Max = 6.5"
Trace Length B – DIMM pin to DIMM pin	Min = 1.1" Max = 1.2"
Trace Length C – Last DIMM pin to parallel termination resistor pad	Min = 0.1" Max = 1.5"
Termination Resistor (R_{TT})	$56 \Omega \pm 5\%$
MCH Breakout Guidelines	5 mil trace width with maximum spacing allowable until beyond the MCH package edge. This breakout length should be as short as possible
Length Tuning Method	MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x# do not require tuning to each other. The lengths are related to the DIMM's associated command clocks. See following section on length requirements.

Figure 6-16. Address/Command Signal Width/Spacing Routing on Lead-in Length

6.2.4.1 Address/Command Group Signal Length Matching Requirements

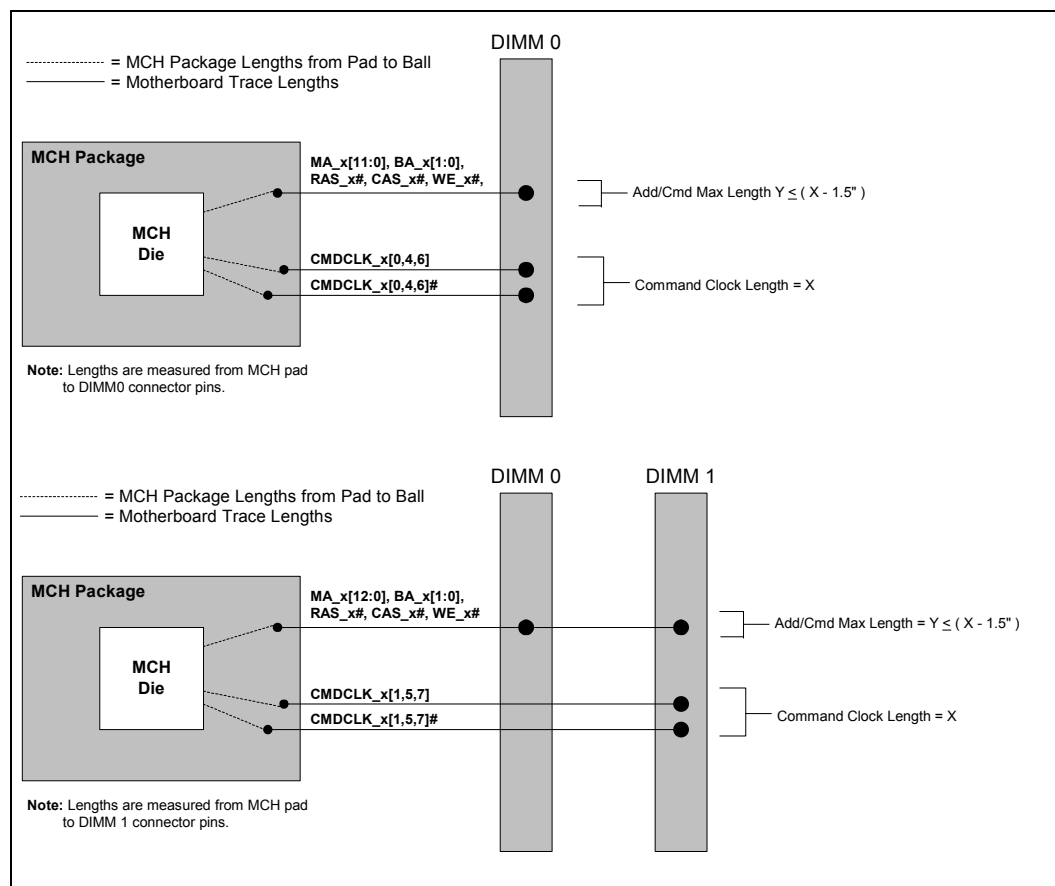
The tuning of the address/command signals ($MA_x[12:0]$, $BA_x[1:0]$, $RAS_x\#$, $CAS_x\#$, $WE_x\#$) and differential clock signals must take into account the internal package lengths of the MCH package. Matching will require tuning of the address/command signals to the differential clock signals from the MCH ball pad to the pins of the DIMM connector. The address/command signals must be routed 1.5 inches or less than the command clock length to the associated DIMM. The address/command signals route to both DIMMs, while the command clocks route only to one respective DIMM. Therefore, the address/command signal length from the MCH die pad to the first DIMM must be 1.5 inches or less than $CMDCLK_x[0,4,6]$ from the die pad to the first DIMM. The address/command signals lengths from the MCH die pad to the second DIMM must be 1.5 inches or less than the $CMDCLK_x[1,5,7]$ lengths. The following equation reiterates the previous text:

$$\begin{aligned} \text{Command Clock Length} &= X, \\ \text{Address/Command Length} &\leq (X - 1.5 \text{ inches}), \end{aligned}$$

No length matching is required from the last DIMM to the parallel termination resistors.

Figure 6-17 shows the length matching requirements between the address/command signals and the clock signals.

Figure 6-17. Address/Command Signal to Command Clock Length Matching Requirements



6.2.5 DC Biasing

6.2.5.1 RCVENOUT_A#, RCVENOUT_B#

The MCH provides two pins, RCVENOUT_A# and RCVENOUT_B#, for Channel A and B, respectively. There is an internal delay loop inside the E7205 chipset package that requires an external termination for the driver. The signal must be tied to a resistor divider between the 2.5 V rail and ground. The high and low side resistor values are shown in Figure 6-18. It is important that the two signal pins do not share a single resistor divider even though the recommended circuit is identical for both. The following figures and table show the recommended topology and layout routing guidelines for the RCVENOUT# signal.

Figure 6-18. DDR Feedback RCVENOUT_A#, RCVENOUT_B# Routing Topology

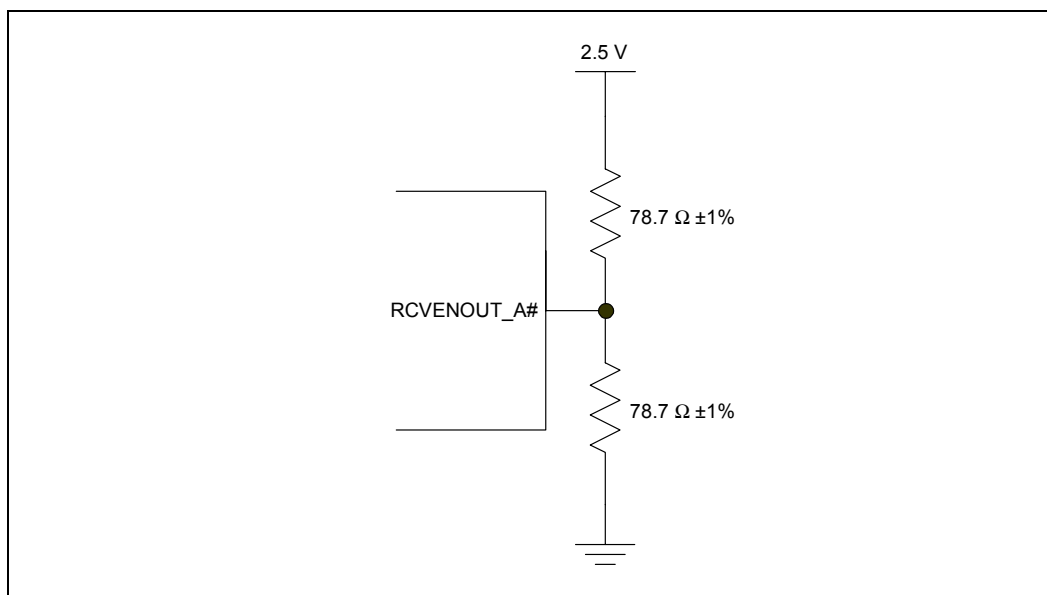


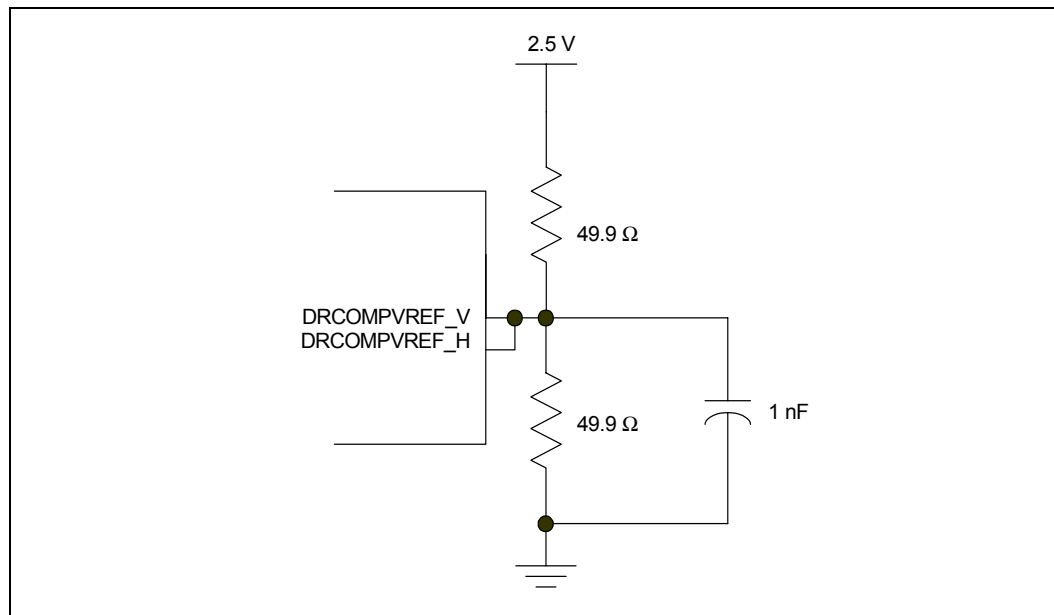
Table 6-11. RCVEN_OUT_A#, RCVENOUT_B# Routing Requirements

Parameter	Routing Guidelines
Signal Group	RCVENOUT_x#
Topology	Point-to-point with resistor divider
Characteristic Trace Impedance	50 Ω
Nominal Trace Width	7 mils
Max Trace Length to Resistor Divider	< 750 mils

6.2.5.2 DRCOMPVREF_H, DRCOMPVREF_V

The MCH provides signals DRCOMPVREF_H and DRCOMPVREF_V for voltage referencing. DRCOMPVREF_H and DRCOMPVREF_V are used for both channel A and B as voltage referencing for the horizontal and vertical buffer resistive compensation circuitry. The DRCOMPVREF_H and DRCOMPVREF_V signals can be shorted together and tied to a single resistor divider network. The values for the biasing circuitry and routing topology are shown in Figure 6-19.

Figure 6-19. DRCOMPVREF_H and DRCOMPVREF_V Routing Topology



NOTE: The capacitor in the figure is 1 nanoFarad.

Table 6-12. DRCOMPVREF_H and DRCOMPVREF_V Routing Requirements

Parameter	Routing Guidelines
Signal Group	DRCOMPVREF_H, DRCOMPVREF_V
Topology	Point-to-point with resistor divider
Nominal Trace Width	20 mils
Resistor Value (Pull-up and Pull-down)	49.9 Ω ± 1%

6.2.5.3 VREF_A and VREF_B

VREF_A and VREF_B are describe in [Section 6.4.4](#).

6.2.5.4 DRCOMP_H and DRCOMP_V

The MCH provides two signals for resistive compensation. The DRCOMP_H and DRCOMP_V signals are used to calibrate the horizontal and vertical DDR buffers, respectively. It is important that these signals do not share biasing circuitry. The individual signal must tie to its own individual resistor which ties to ground. The values for the biasing circuitry and routing topology are provided in [Figure 6-20](#) and [Table 6-13](#).

Figure 6-20. DRCOMP_H and DRCOMP_V Routing Topology

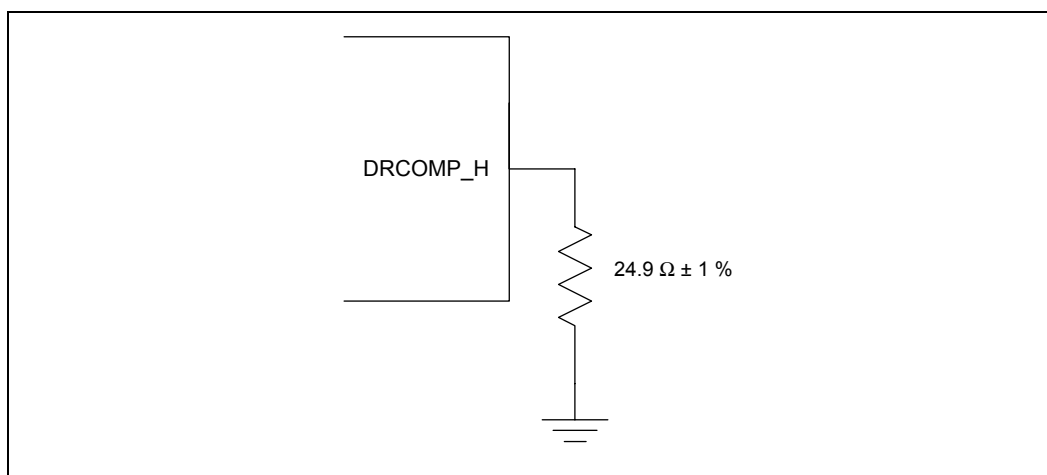


Table 6-13. DRCOMP_H and DRCOMP_V Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DRCOMP_H, DRCOMP_V
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Characteristic Trace Impedance (Z_0)	50 Ω
Nominal Trace Width	7 mils
Resistor Value	24.9 $\Omega \pm 1\%$
Max Trace Length to Resistor Divider	< 750 mils

6.2.5.5 DDR_STRAP

The MCH provides a signal that is used to indicate to the BIOS the type of memory that is implemented in a motherboard design. This signal should be pulled to 2.5 V. The topology is shown below.

Figure 6-21. DDR_STRAP Routing Topology

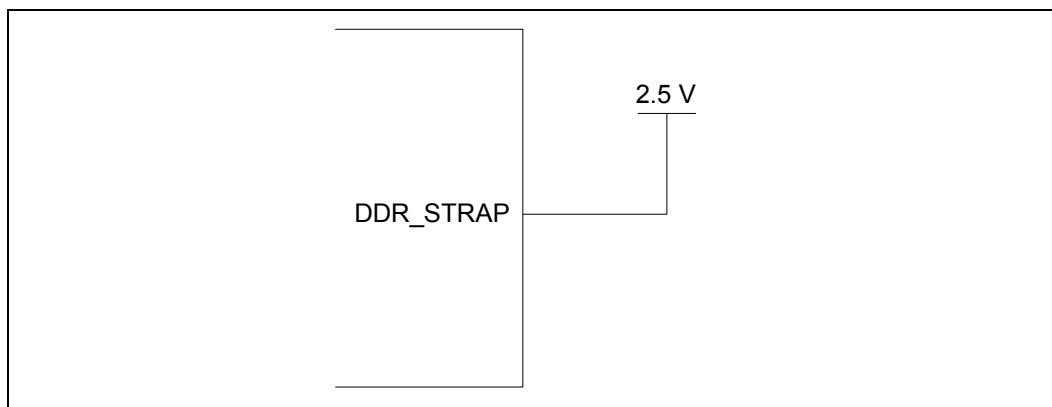


Table 6-14. DDR_STRAP Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DDR_STRAP
Topology	Float or point-to-point with pull-down resistor
Nominal Trace Width	7 mils

6.2.5.6 ODTCOMP

The MCH provides a signal that is used to tune the on-die termination resistors on the DDR interface. This signal should be tied ground through a resistor. The topology and resistor value is shown in Figure 6-22.

Figure 6-22. ODTCOMP Routing Topology

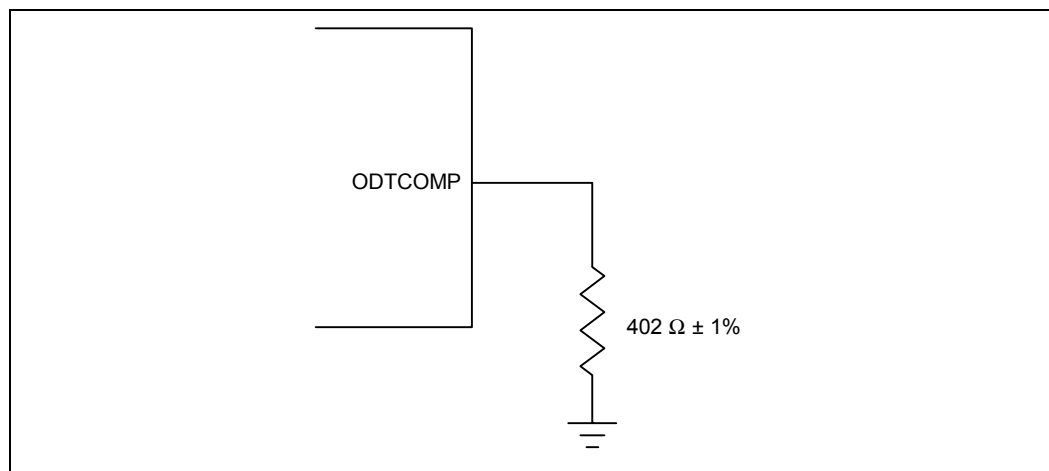


Table 6-15. ODTCOMP Routing Requirements

Parameter	Routing Guidelines
Signal Group	ODTCOMP
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Resistor Value	$402\ \Omega \pm 1\%$
Characteristic Trace Impedance (Z_0)	$50\ \Omega$
Nominal Trace Width	7 mils
Max Trace Length Limit to Resistor	< 750 mils

6.3 System Memory Bypass Capacitor Guidelines

6.3.1 MCH System Memory Interface Decoupling Requirements

6.3.1.1 MCH System Memory High-Frequency Decoupling

Every MCH ground and power ball in the system memory interface should have its own via. For 2.5 V high-frequency decoupling, a minimum of ten 0603 0.1 μ F high-frequency capacitors are required and must be within 100 mils of the MCH package. The vias should be placed within 25 mils of the capacitor pads. The traces from the ground and power vias to the capacitor pad must be as wide as possible. Figure 6-23 shows the MCH DDR 2.5 V high-frequency decoupling capacitors.

Figure 6-23. MCH DDR 2.5 V Decoupling

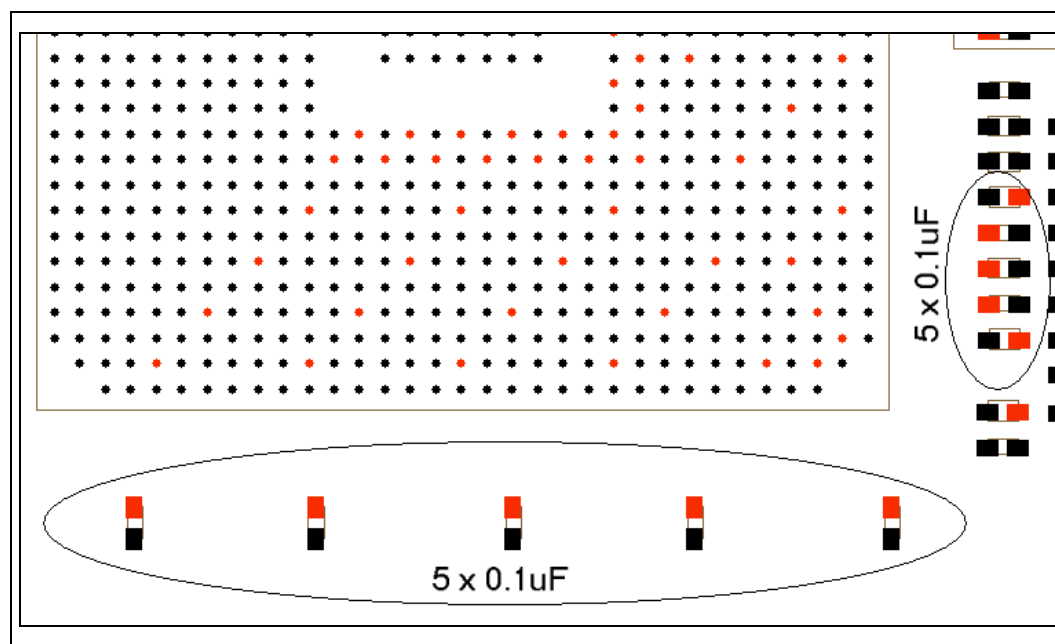


Table 6-16. MCH System Memory Decoupling Capacitor Requirements

Parameter	Guideline
Capacitor Number	Ten 0603 0.1 μ F MLC capacitors placed near MCH
Capacitor Placement	Within 100 mils of the MCH
Capacitor Pad to Ground via Trace Width	Route as wide as possible with a minimum width of 18 mils
Vias (Power and Ground)	Placed within 25 mils of the capacitor pad

6.3.1.2 MCH System Memory Low-Frequency Bulk Decoupling

The MCH system memory interface requires low-frequency bulk decoupling. Place four 100 μ F electrolytic capacitors between the MCH and the first DIMM connector. These capacitors are in addition to the bulk decoupling required by the 2.5 V regulator (regulator bulk decoupling is design specific).

Figure 6-24. Shared MCH/DIMM 2.5 V Bulk Decoupling Example

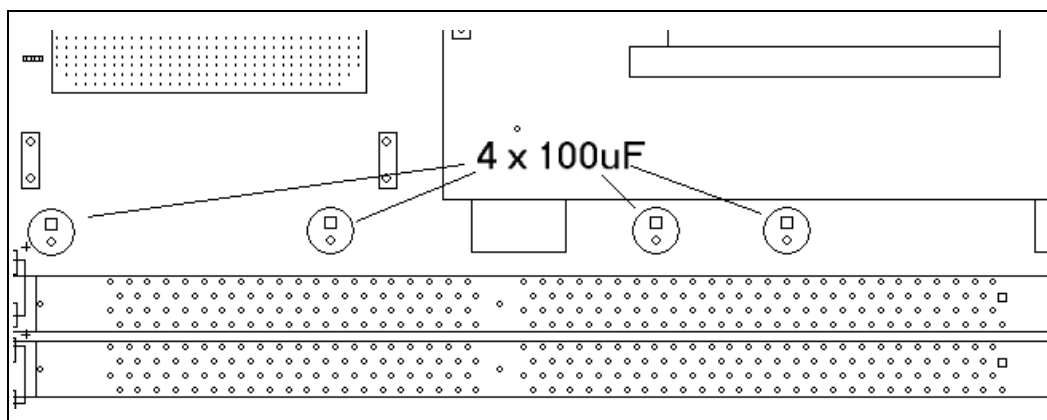


Table 6-17. MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Four 100 μ F capacitors
Capacitor placement	Evenly placed between the MCH and first DIMM pin

6.3.2 DDR-DIMM Decoupling Requirements

The DDR DIMMs require bulk decoupling in addition to the decoupling that is required by the MCH. Place two 100 μ F capacitors per DIMM at each end. A 4-DIMM design would use eight total 100 μ F caps. Using a 7343-sized capacitor will allow placement under the lever actuated arms of the DIMMs.

Figure 6-25. DIMM Bulk Capacitor Requirements

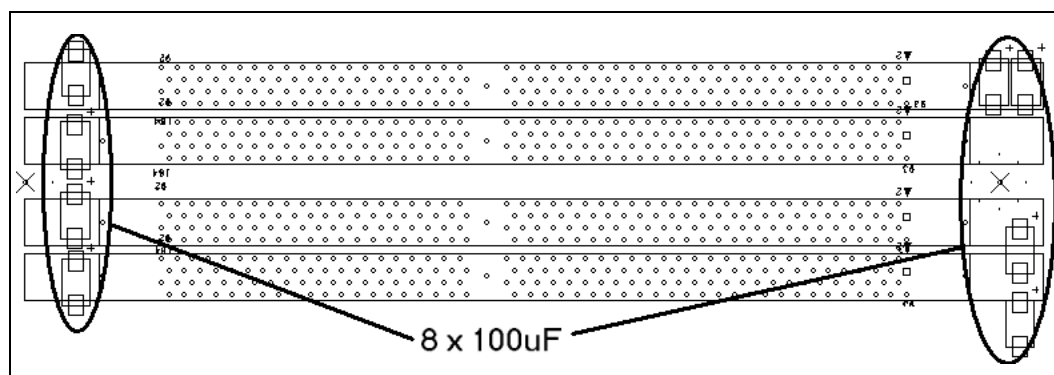


Table 6-18. DIMM Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Two 100 μ F capacitors per DIMM
Capacitor placement	One placed at both the left side and the right side of the DIMM sockets

6.4 Power Delivery

The following guidelines are recommended for an E7205 chipset DDR system memory design. The main focus of these MCH guidelines is to minimize signal integrity problems and improve the power delivery of the MCH system memory interface and the DDR-DIMMs.

6.4.1 DDR Voltage Regulator Guidelines

E7205 chipset designs using the DDR-SDRAM memory sub-system require several different voltages: 2.5 V, 1.25 V, and VREF. To generate these voltages, a 2.5 V and a 1.25 V regulator are required and must be designed to supply the required voltage and current levels to meet both the MCH and the DDR-SDRAM device requirements. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to the needs of different OEM design targets.

6.4.2 Power Delivery Guidelines for 2.5 V

Attention must be paid to the 2.5 V power plane to ensure proper MCH and DIMM power delivery. This 2.5 V plane must extend from the MCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V power plane under the DIMM connectors must encompass all of the DIMM 2.5 V pins.

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the MCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V Core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

6.4.3 Power Delivery Guidelines for 1.25 V

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (VTT). Special considerations must be taken for the 1.25 V regulator design because it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

6.4.4 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the MCH to compare the input data signal levels. VREF must be generated as shown in the [Figure 6-26](#). It should be generated from a typical resistor divider using 1%-tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the DIMMs. Additionally, VREF must be decoupled locally at each DIMM connector and at the MCH. Finally, the VREF signal should be routed with as wide a trace as possible (12 mils minimum width), and isolated from other signals with a minimum of 12 mils spacing. During breakout from the MCH, a minimum of 7 mil spacing can be maintained for a maximum length of 350 mils.

Figure 6-26. DDR VREF Generation Example Circuit

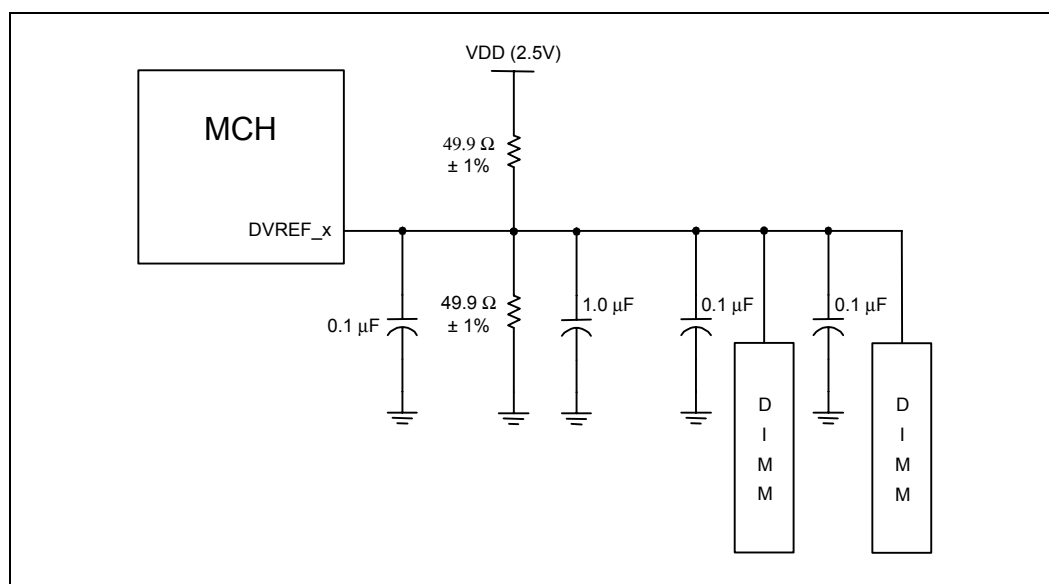


Table 6-19. DDR VREF Generation Requirements

Parameter	Guideline
VREF Routing	Minimum 12 mils wide and separated from other traces with a minimum 12 mils spacing, except during breakout, which is allowed 7 mil spacing to other signals for no more than 350 mils.
Voltage Divider	Place resistor divider consisting of two $49.9\ \Omega \pm 1\%$ resistors. Minimize distance from MCH to resistor divider.
Decoupling Requirements	Three 0603 0.1 μF capacitors One 0603 1.0 μF capacitor
Decoupling Placement	Place one 0.1 μF decoupling cap at each of the DIMM sockets, and one 0.1 μF decoupling cap at the MCH. Place the 1.0 μF decoupling cap near the voltage divider.

6.4.5 DDR VTT Termination

All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the MCH. Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector. The VTT termination island must be at least 50 mils wide. Use this termination island to terminate all DDR signals using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK are from the same DDR signal group. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT island on the top signal layer.

Figure 6-27. DDR VTT Termination Island Example

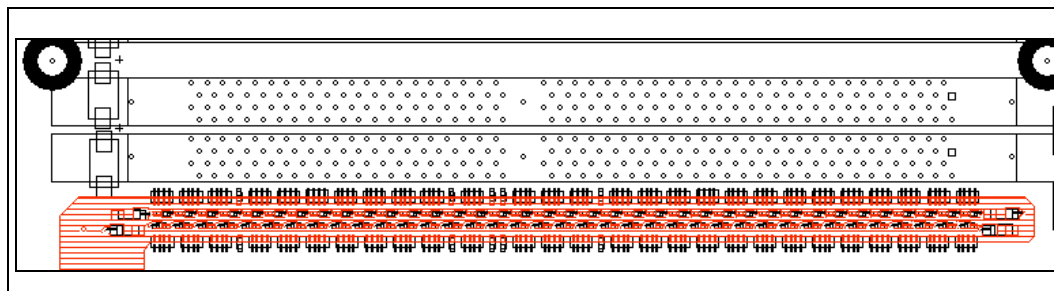


Table 6-20. DDR VTT Termination Island Requirements

Parameter	Guideline
Island Width	50 mils minimum
Resistor and capacitor connectivity	Connect termination resistors and decoupling capacitors directly to the termination island

6.4.5.1 VTT Termination Island High-Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors—one 0603 0.1 μF capacitor per two DDR signals, or two capacitors per RPACK. These decoupling capacitors connect directly to the VTT island and to ground, and must be spread-out across the termination island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via should be within 25 mils of the capacitor pad and the via, and the pad should be connected with as wide a trace as possible. The distance from any DDR termination resistor pin to a 0.1 μF VTT capacitor pin must not exceed more than 100 mils.

Finally, place two 4.7 μF ceramic capacitors on each end of the termination island (see Figure 6-30).

Figure 6-28. DDR VTT Termination 0.1 μF High-Frequency Capacitor Example 1

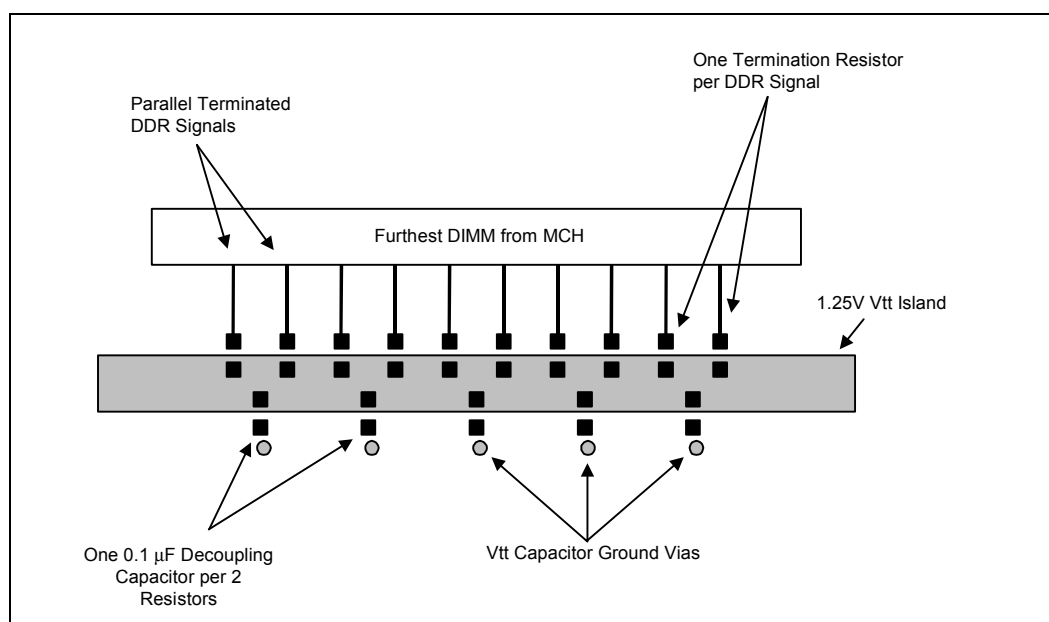


Figure 6-29. DDR VTT Termination and High-Frequency Capacitor Example 2

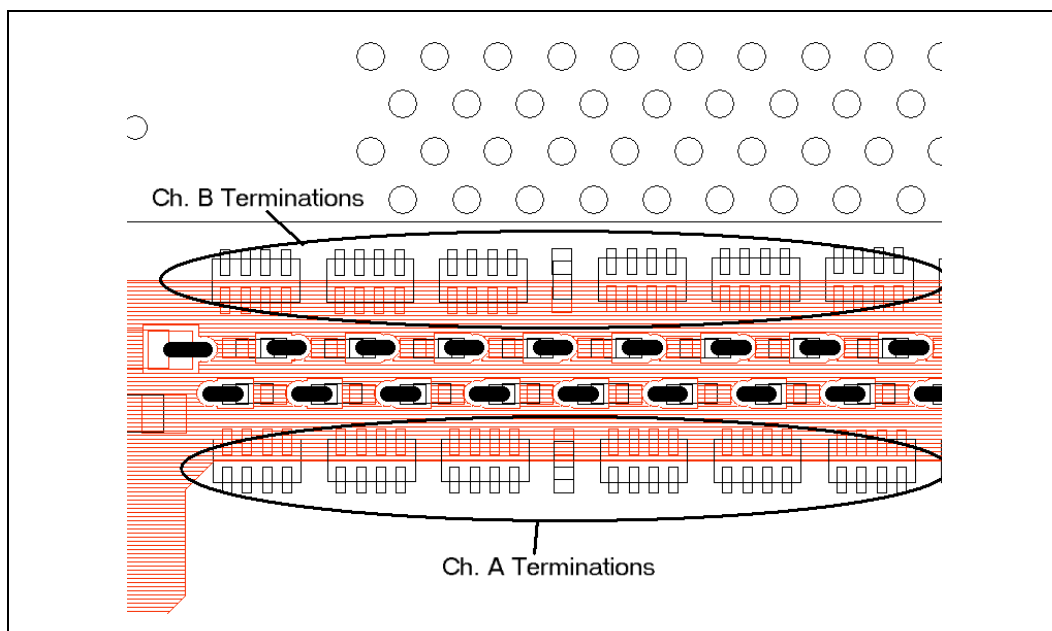


Figure 6-30. DDR VTT Termination 4.7 μ F High-Frequency Capacitor Example

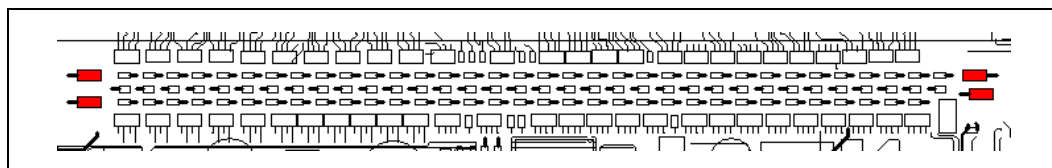


Table 6-21. DDR VTT Termination Island High-Frequency Decoupling Requirements

Parameter	Guideline
0.1 μ F capacitors	Place one decoupling cap for every two DDR signals/termination resistors (or two caps for every RPACK). The distance from any termination resistor to decoupling capacitor should not exceed 100 mils.
4.7 μ F capacitors	Four capacitors required. Place two capacitors at each end of the termination island.

6.4.5.2 VTT Termination Island Low-Frequency Bulk Decoupling Requirements

The VTT termination island requires low-frequency bulk decoupling. The output of the 1.25 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25 V regulator will vary according to the needs of specific OEM design targets.

6.4.6 Power Sequencing Requirements

6.4.6.1 MCH Power Sequencing Requirements

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset. Common design practice is to have all MCH power rails come up as close in time as possible.

6.4.6.2 DDR-SDRAM Power Sequencing Requirements

There are no DDR-SDRAM power sequencing requirements except that 1.25 V must come up after the 2.5 V rail. Because of this requirement, designs should have the 1.25 V rail derived from a regulator with 2.5 V as its input.

Hub Interface 1.5

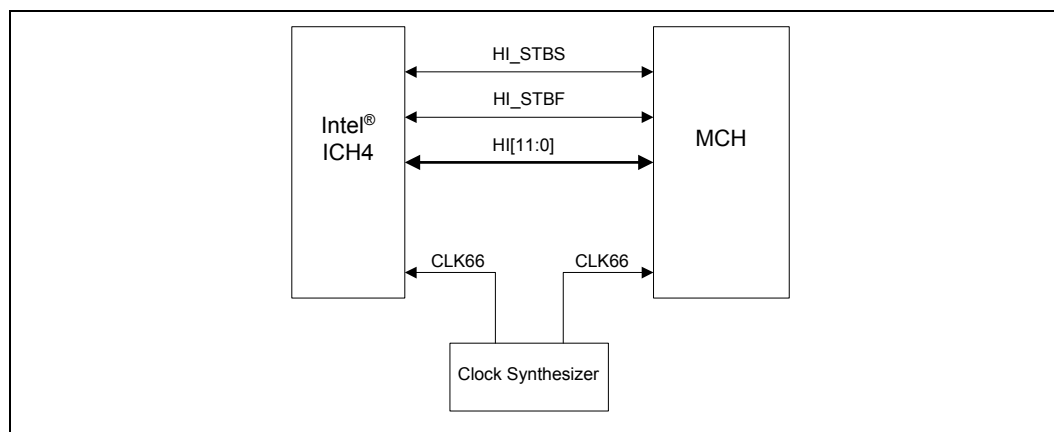
7

This chapter describes the routing guidelines for the 8-bit hub interface 1.5. This hub interface connects the MCH to the ICH4 (see [Figure 7-1](#)). This interface supports only the parallel termination mode. Therefore, the DPRSLPVR pin on the ICH4 must be tied to ground to ensure that it will run in parallel mode.

The MCH and ICH4 ball assignments are optimized to simplify the hub interface routing between these devices. The hub interface signals must be routed directly from the MCH to the ICH4 with all signals referenced to VSS. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The 8-bit hub interface signals are all in the same data group (i.e., all signals are associated with HI_STBS/HI_STBF).

Figure 7-1. 8-Bit Hub Interface 1.5 Routing



7.1 Hub Interface 1.5 High-Speed Routing Guidelines

The Hub Interface 1.5 signal groups are listed in [Table 7-1](#). The general routing parameters for the HI 1.5 signals are listed in [Table 7-2](#).

Table 7-1. HI 1.5 Signal Groups

Group	Signals
Common Clock Signal	HI_x[11:8]
Source Synchronous Signal	HI_x[7:0], HI_STBF, HI_STBS
Miscellaneous Signal	HIRCOMP, HISWNG, HIVREF

Table 7-2. HI 1.5 Routing Parameters

System Type	Trace Length Min-Max	Trace Z_0	Trace Width/Spacing	Breakout Width/ Spacing
266 MT/s	3"–20"	$50 \Omega \pm 10\%$	Data to Data: 7/13 mils Strobe to Strobe: 7/13 mils Strobe to Data: 7/18 mils Other signals to Data: 7/13 mils	7/5 mils at MCH (max dist = 750 mils) 7/5 mils at Intel® ICH4 (max dist = 500 mils)

Each strobe signal trace must be the same length for HI 1.5 devices on the motherboard, and each data signal trace must be matched within ± 100 mils.

7.2 Hub Interface 1.5 Generation/Distribution of Reference Voltages

The nominal Hub Interface 1.5 reference voltage is $0.35 \text{ V} \pm 5\%$. The 8-bit hub interface on the MCH has a dedicated HIVREF pin to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal hub interface 1.5 reference voltage swing must be 0.8 V for the MCH and ICH4. Each hub interface on the MCH has a dedicated HISWNG pin to sample this reference swing voltage. The ICH4 also has a dedicated reference swing voltage pin (HITERM). Refer to the [Table 7-3](#). Both of these reference voltages can be generated locally with a single voltage divider circuit. [Figure 7-2](#) shows an example voltage divider circuit.

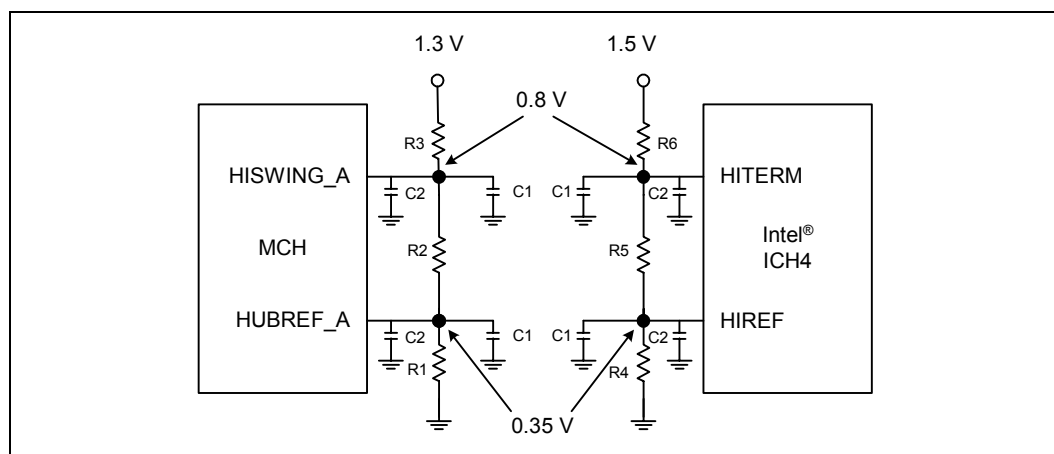
Table 7-3. HI 1.5 Reference Circuit Specifications

Reference Voltage Specification (V) (HIREF)	Reference Swing Voltage Specification (V) (HITERM)	1.3 V Voltage Divider Circuit Recommended Values	1.5 V Voltage Divider Circuit Recommended Values	
			Group 1 ¹	Group 2 ¹
$0.350 \pm 5\%$	For Intel® ICH4 = 0.8 For MCH = 0.8	R1 = $402 \Omega \pm 1\%$ R2 = $511 \Omega \pm 1\%$ R3 = $549 \Omega \pm 1\%$ C1 = $0.1 \mu\text{F}$ C2 = $0.01 \mu\text{F}$	R6 = $80.6 \Omega \pm 1\%$ R5 = $51.1 \Omega \pm 1\%$ R4 = $40.2 \Omega \pm 1\%$ C1 = $0.1 \mu\text{F}$ C2 = $0.01 \mu\text{F}$	R6 = $226 \Omega \pm 1\%$ R5 = $147 \Omega \pm 1\%$ R4 = $113 \Omega \pm 1\%$ C1 = $0.1 \mu\text{F}$ C2 = $0.01 \mu\text{F}$

NOTE:

1. Use only resistors from group 1 or 2—do not mix values from these groups.

Figure 7-2. HI 1.5 Locally Generated Reference Divider Circuits



All resistor values must be rated at $\pm 1\%$ tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A $0.1 \mu\text{F}$ capacitor (C1 in [Figure 7-2](#)) should be placed close to each resistor divider, and a $0.01 \mu\text{F}$ bypass capacitor (C2 in [Figure 7-2](#)) should be placed within 0.25 inches of reference voltage pins. The trace length from the voltage divider circuit to the HIREF and HUBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

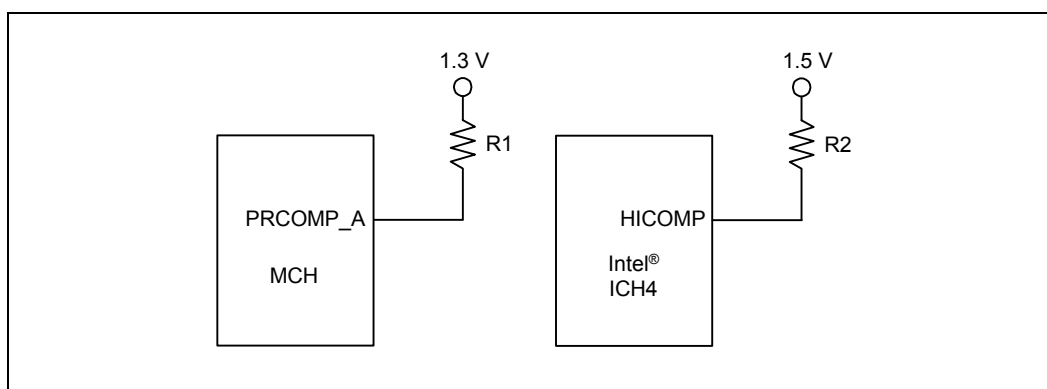
7.3 Hub Interface 1.5 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

Table 7-4. Hub Interface 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 $\Omega \pm 10\%$	R1 = 32.4 $\Omega \pm 1\%$	VCC1_3
Intel® ICH4	50 $\Omega \pm 10\%$	R2 = 43.3 $\Omega \pm 2\%$	VCC1_5

Figure 7-3. Hub Interface 1.5 RCOMP Circuits



7.4 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 μF capacitors per each component (i.e., the ICH4 and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_5/VCC1_3 side of the capacitors to the VCC1_5/VCC1_3 power pins. Similarly, if layout allows, metal fingers running on the VCC1_5/VCC1_3 side of the board should connect the ground side of the capacitors to the VSS power pins.

Serial ATA

8

This chapter provides guidelines for integrating discrete high-speed Serial ATA onto systems based on the E7205 chipset using ICH4. The topics discussed include layout and routing guidelines, and platform integration.

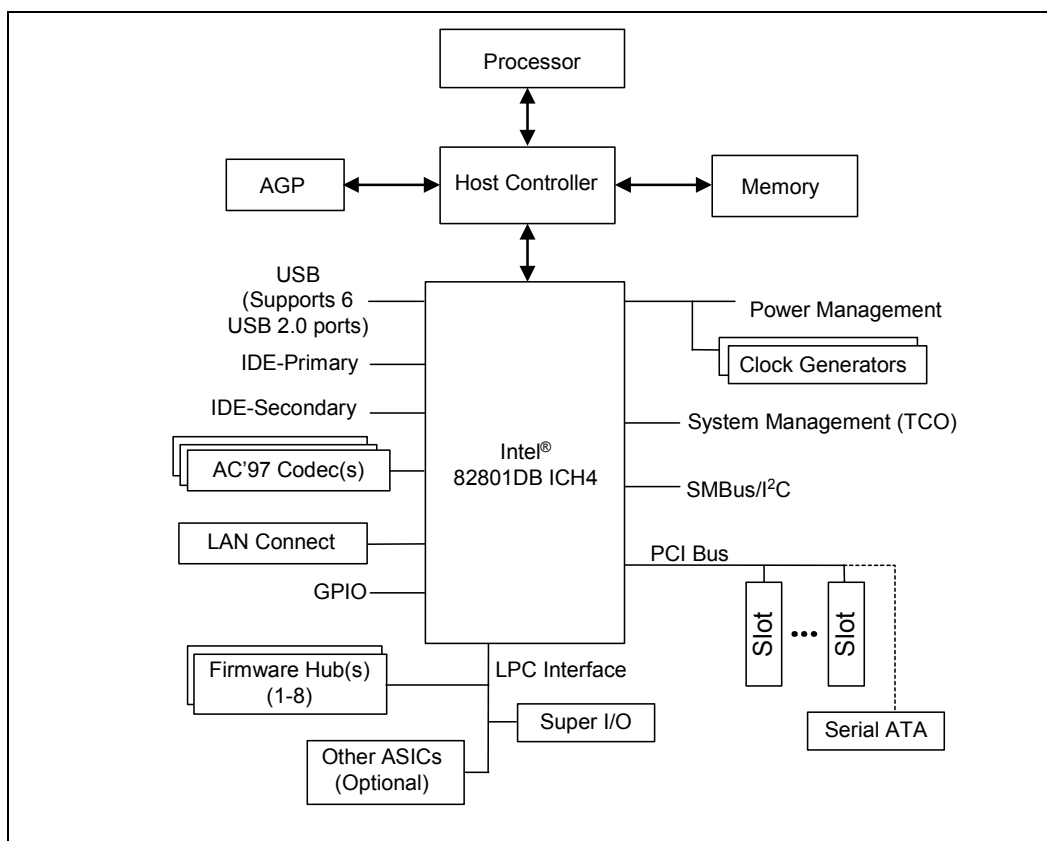
Note: The guidelines recommended in this chapter are based on experience and simulation work performed at Intel while developing Serial ATA. This work is ongoing, and the recommendations and considerations are subject to change. [Table 8-1](#) shows a comparison of the Serial ATA (Gen I) and Parallel ATA technologies.

Table 8-1. Serial ATA vs. Parallel ATA

Parameter	Serial ATA	Parallel ATA
Performance	150 MB/s	100 MB/s
Max Cable Length	39.37 inches	18 inches
Signaling Tolerance	250 mV	5 V
Signal pins on cable	4	26

Figure 8-1 shows the Serial ATA solution using a discrete host controller.

Figure 8-1. Uni-Processor System Block Diagram (Intel® ICH4) with Serial ATA



8.1 Host Controller Details

The E7205 chipset platform will use the Sil3112* device from Silicon Image. This section gives details on package type, mechanical specifications, function, and general layout of the part.

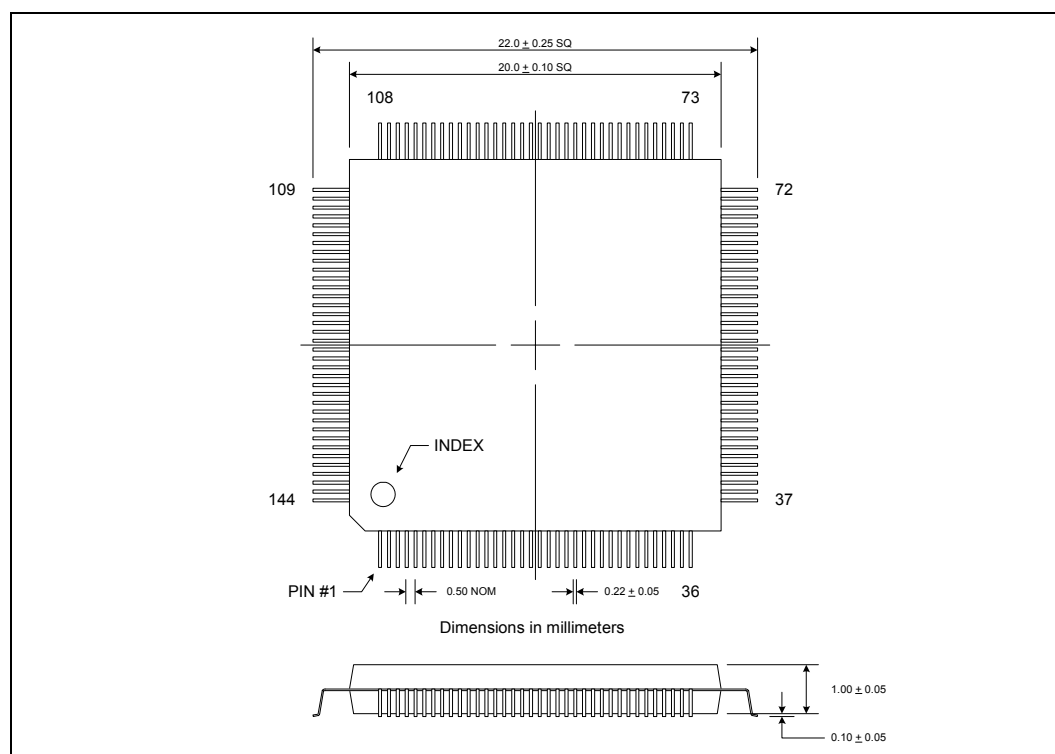
8.1.1 Functional Description

The Sil3112 is a PCI-to-Serial ATA controller chip that transfers data between the PCI bus and storage media. The Sil3112 communicates with the ICH4 over the PCI bus, and communicates with storage media over the Serial ATA bus.

Note: The Sil3112 PCI interface is compliant with *PCI Local Bus Specification (Revision 2.2)*.

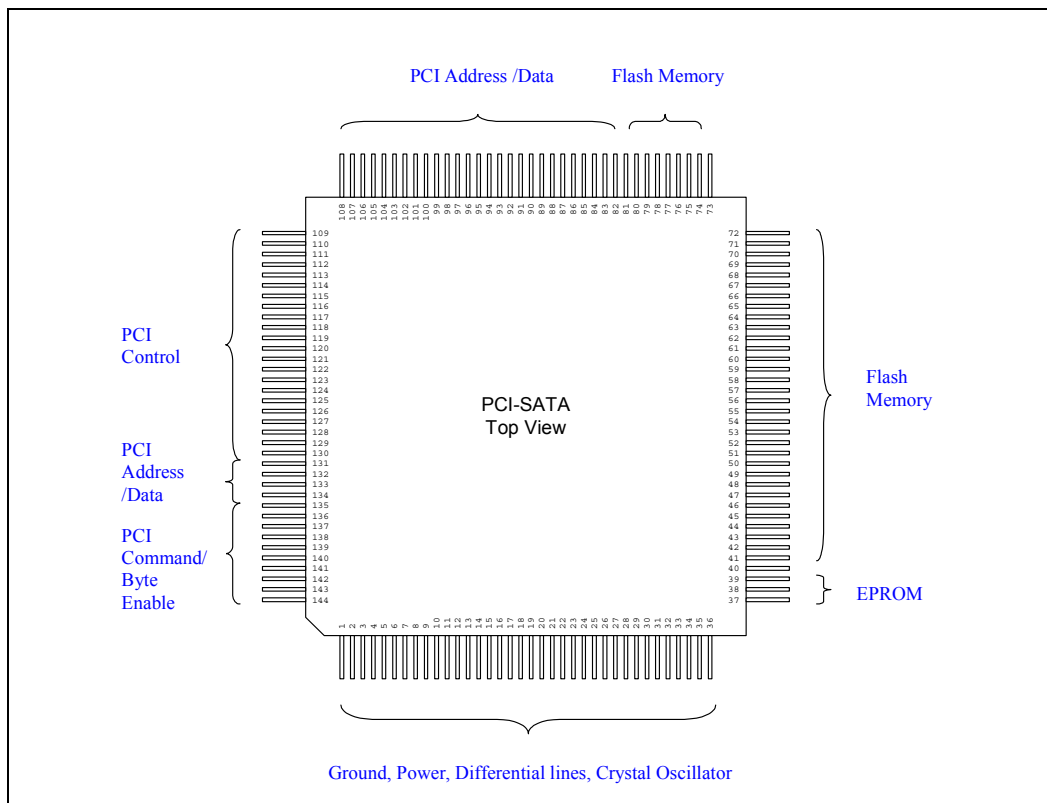
8.1.2 Mechanical Specifications

Figure 8-2. Host Controller Mechanical Specifications (144-pin TQFP Package Type)



8.1.3 Quadrant Layout

Figure 8-3. Quadrant Layout of the Host Controller



8.2 Layout/Routing Guidelines

8.2.1 General Recommendations

8.2.1.1 Ground Planes

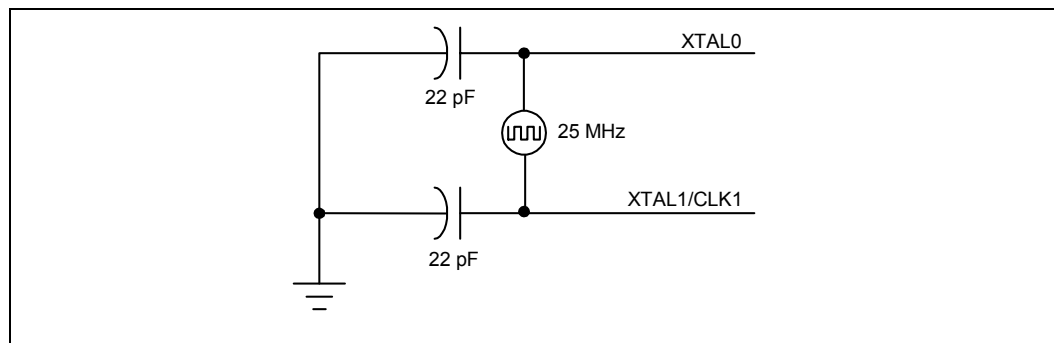
Considerations for designing the ground planes around differential lines:

- The ground plane over/under the differential traces should be a continuous plane from chip ground to connector ground.
- Any discontinuity or a split of the ground plane should be avoided.
- The ground plane should have ground contact to both the chip analog ground (pin numbers 8, 11, 14, 17, 21, 24, 27, 30, 34), and at connector ground.
- The ground plane should extend more than twice the width of the signal trace beyond the differential pair.

8.2.1.2 Clock Topology

The Serial ATA device requires a 25 MHz crystal in combination with its own PLLs. A 22 pF capacitor to each of the clock pins (XTAL0, XTAL1) is recommended.

Figure 8-4. Example of Clock Implementation



8.2.2 Routing Constraints

This section describes critical considerations for routing signals and power to the chip and connector. Three of the topics discussed are stack-up, trace length, and connector placement.

8.2.2.1 6-Layer Stack-Up PCB

Figure 8-5. Microstrip PCB Stack-Up

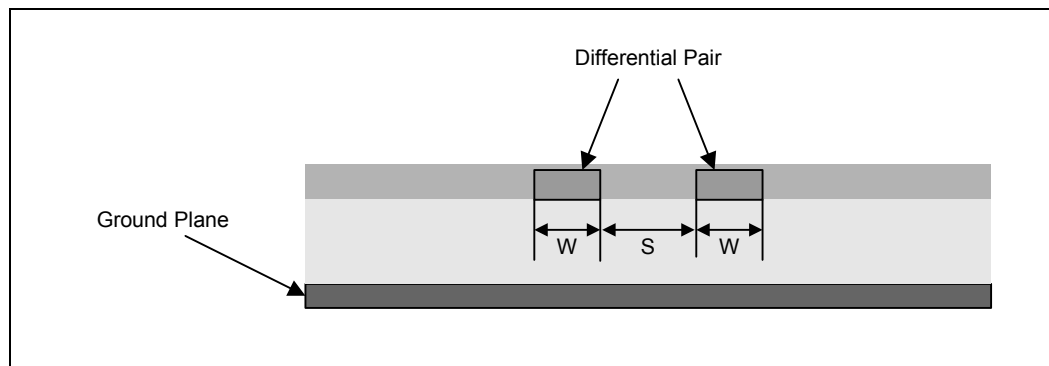


Table 8-2. Microstrip PCB Stack-Up

Parameter	Value
S (Separation between differential pair)	7 mils
W (width of transmission line)	5 mils
$Z_o = Z_{11}$	58 Ω
Z_{diff} (Differential Line Impedance)	100 $\Omega \pm 5 \Omega$

8.2.2.2 Differential Lines Discussion

8.2.2.2.1 Length

The length of the differential pairs (Tx pair and Rx pair) should be as short as possible. The recommended maximum length constraint is 3.9 inches. If the maximum length is exceeded, the high-frequency differential signal will suffer signal attenuation and increased rise time/fall time.

8.2.2.2.2 Length Matching

The two traces in a differential pair should be matched in length. The lines should have same line length, number of vias, transmission line structure, and pad sizes. The traces in a differential pair should match in length within 17.72 mils. The 17.72 mils difference of the signal propagation produces about 3 ps skew.

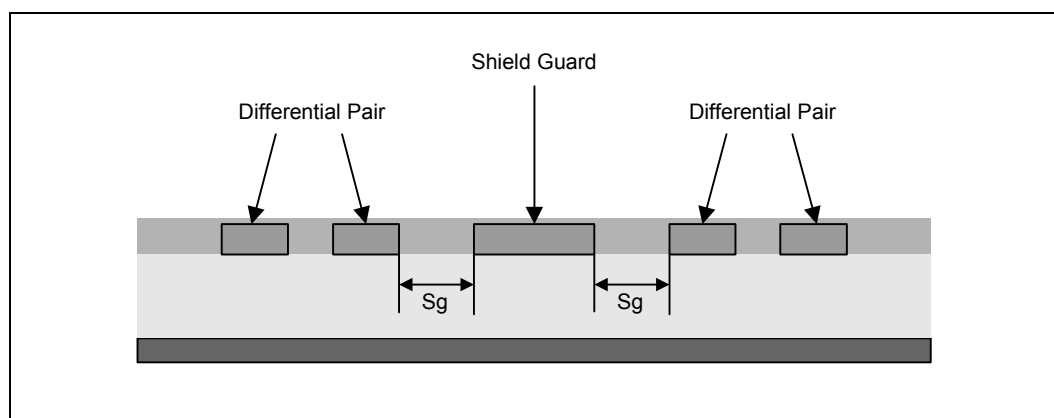
8.2.2.2.3 Pads and Stubs

The size of the soldering pads on the differential pair should be small to reduce the parasitics of the pads. It is recommended to keep the pad size 60 mils x 30 mils or smaller. This will enable the parasitic capacitance of a bonding pad to be kept below 50 pF. The capacitance loading effect of the conventional pad (with ground plane under the pad) is not acceptable. Hence, the ground plane under the bonding pad must be removed. The effect of other metals on the opposite side of the PCB core can be ignored because the thickness of the core is 40 mils, which is relatively thick. Stubs should be avoided on the differential lines.

8.2.2.2.4 Crosstalk

To reduce the crosstalk noise between the nearby differential pairs or to other adjacent signal lines, grounded shield guard can be inserted between the pairs or before the adjacent lines to the differential pairs. To improve the effect of the shields, the shield guard should be grounded at the chip and at the Serial ATA connector. Figure 8-6 shows the grounded shield guard for the microstrip line structure. It is recommended that $S_g \geq 2W$, where W is width of the differential signal trace.

Figure 8-6. Grounded Shield Guard



8.2.3 Layout Routing Strategy

8.2.3.1 Routing of Differential Lines

The two routing examples for Sil3112 and the Serial ATA connector are shown in [Figure 8-7](#), [Figure 8-8](#), [Figure 8-9](#) and [Figure 8-10](#). [Figure 8-7](#) and [Figure 8-8](#) are examples of vertical orientation of the Serial ATA connectors, while [Figure 8-9](#) and [Figure 8-10](#) are examples of horizontal orientation of the Serial ATA connectors. In the figures, differential pairs (Tx, Rx) are connected between the Sil3112 chip and the Serial ATA connectors.

Figure 8-7. Serial ATA Connectors (Vertical Orientation Example 1)

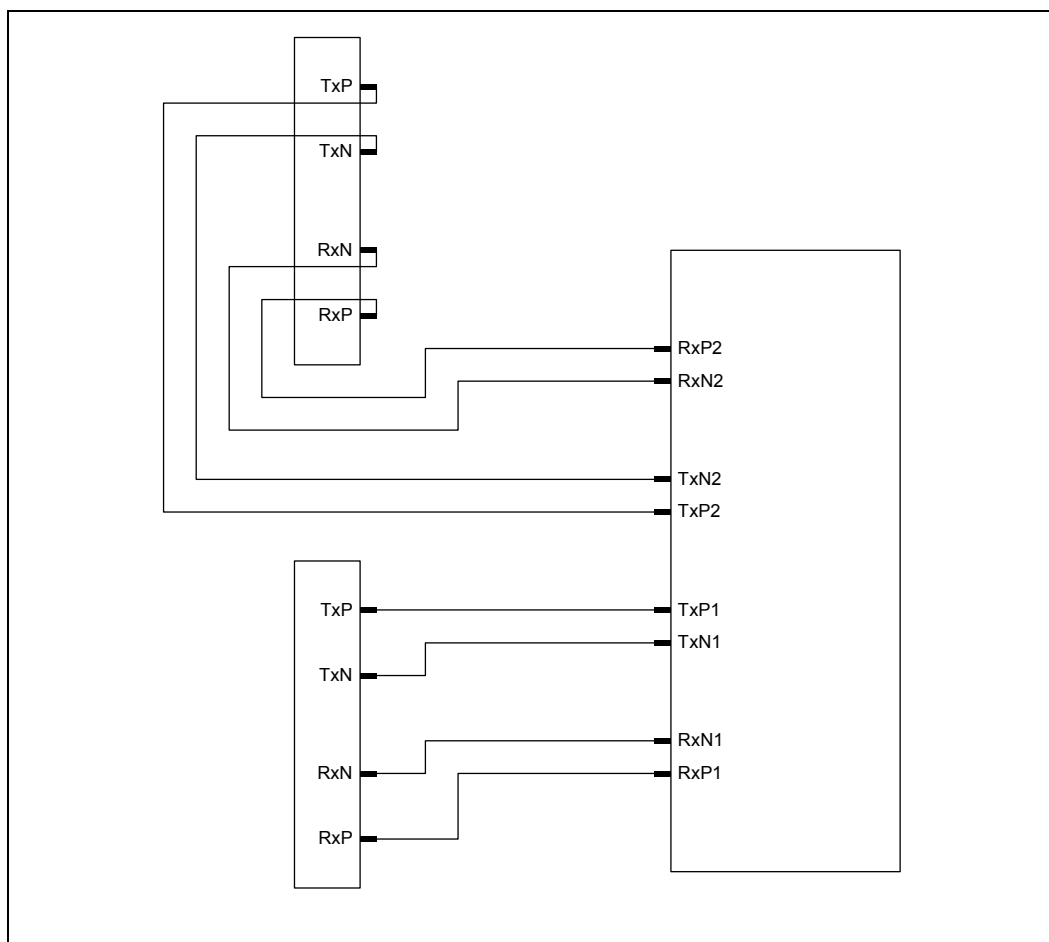


Figure 8-8. Serial ATA Connectors (Vertical Orientation Example 2)

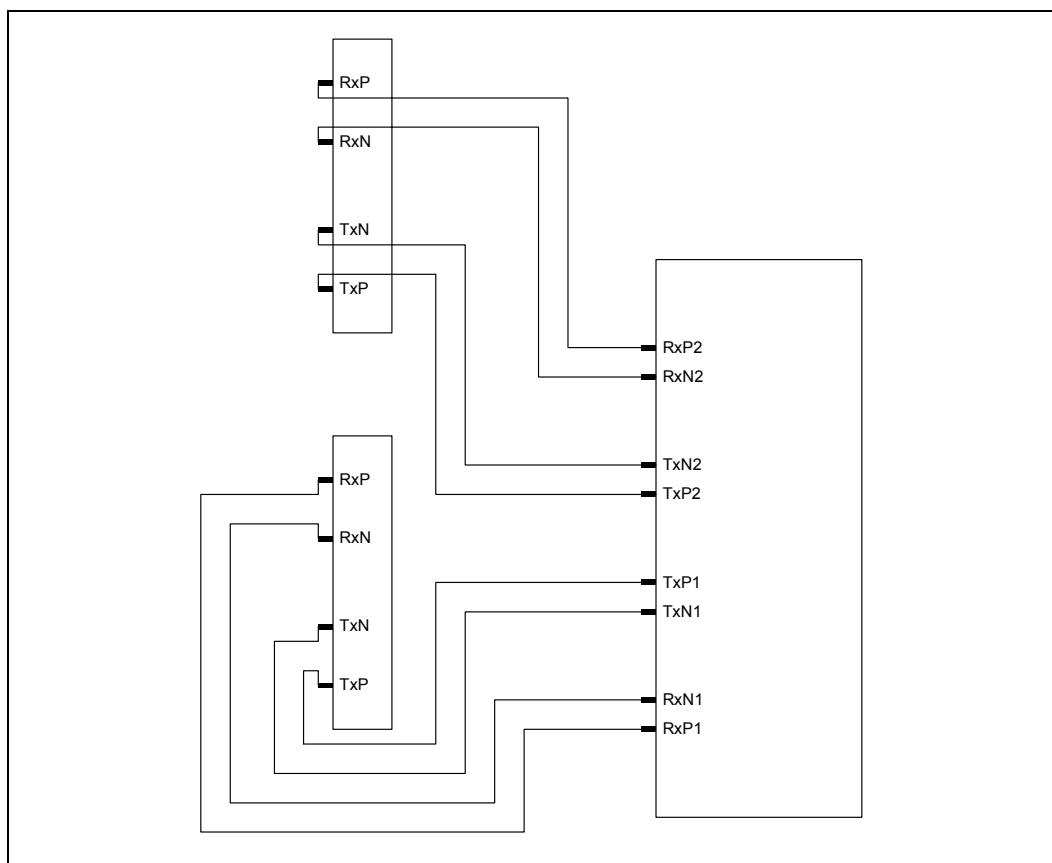


Figure 8-9. Serial ATA Connectors (Horizontal Orientation Example 1)

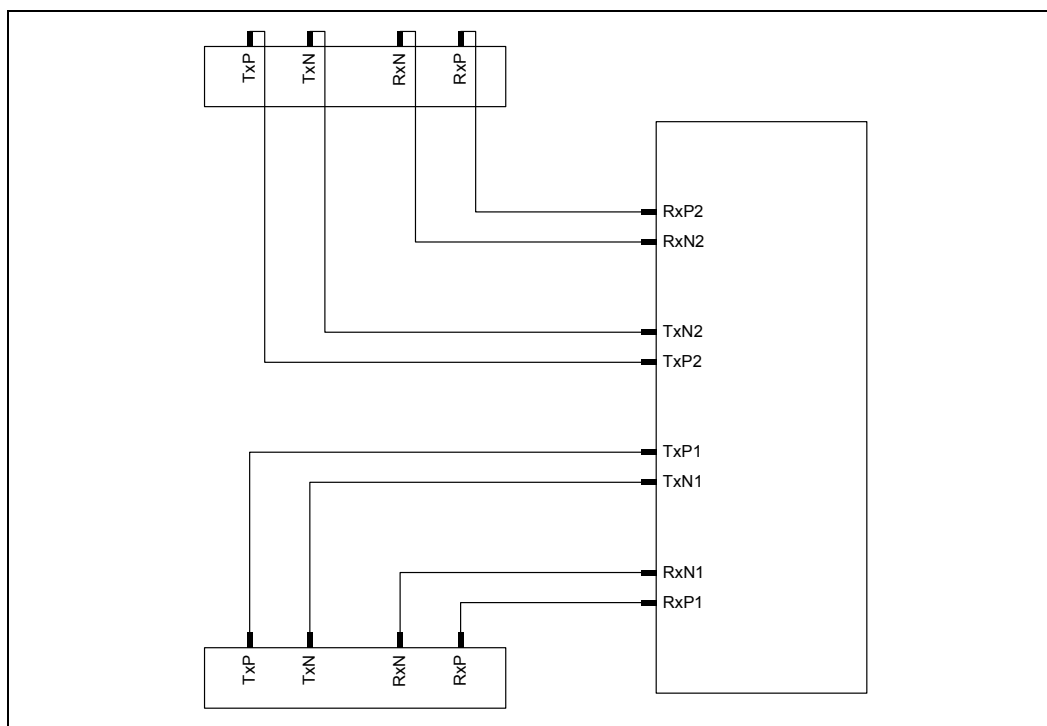
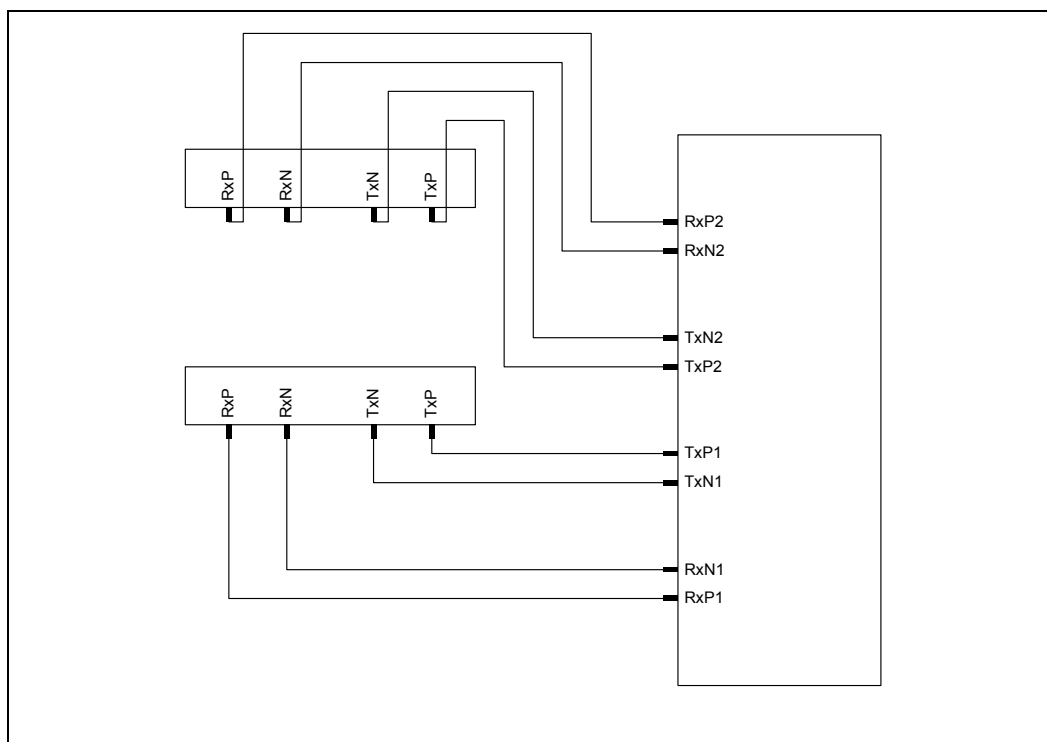


Figure 8-10. Serial ATA Connectors (Horizontal Orientation Example 2)



8.3 Platform Integration Considerations

8.3.1 Power Supply Considerations

8.3.1.1 Voltages

The voltages that are supplied to the controller are 1.8 V and 3.3 V. The 3.3 V pins are used to supply power to I/O, which have a tolerance of ± 0.3 V. The 1.8 V pins supply power to the internal core and SerDes power.

8.3.1.2 Power Consumption

The estimated typical power consumption for the Sil3112 is shown in [Table 8-3](#).

Table 8-3. Typical Power Consumption

Voltage	Current
1.8 V Supply current for PHY blocks	190 mA
1.8 V Supply current for core logic	140 mA
3.3 V Supply current (for I/Os)	55 mA

8.3.1.3 Decoupling

The recommended number of decoupling capacitors for the 3.3 V signal rail is eleven. Each of these capacitors should have a value of 0.1 μ F. For the 1.8 V signal rail it is recommended to use ten 0.1 μ F capacitors and one 10 μ F capacitor. In all these cases the capacitor should be placed as close as possible to the package. When choosing these components, the smallest components should be chosen since they have the least parasitic inductance.

Optional solder pads for coupling capacitors are recommended both for Tx and Rx serial lines. For DC coupling case, a 0 Ω resistor can be placed between these pads. For AC coupling, 0.01 μ F ceramic capacitors can be used. When placing solder pads for coupling capacitors, minimum solder pad size should be used. No stubs from the Tx/Rx lines are allowed.

To improve the decoupling capability of the small decoupling capacitors (0.1 μ F or 0.01 μ F), LIC (Low Inductance Capacitor) can be used with BGA type bonding. These decoupling capacitors can be placed between GND and VDD, and the soldering pads should be small.

8.3.1.4 Power Supply Isolation for Analog Blocks

Table 8-4. Differential Pin Description

Pin #	Pin Name	Function
6	VDDD	Rx power
12	VDDD	Tx power
19	VDDD	PLL power
25	VDDD	Tx power
32	VDDD	Rx power
37	VDDD	Xtal power

These power pins supply internal analog and clock generation blocks. They are sensitive to power supply noise. Attention should be paid to proper isolation and bypassing of these pins. [Figure 8-11](#) shows the recommended circuitry.

Figure 8-11. Example Circuitry for Analog Blocks

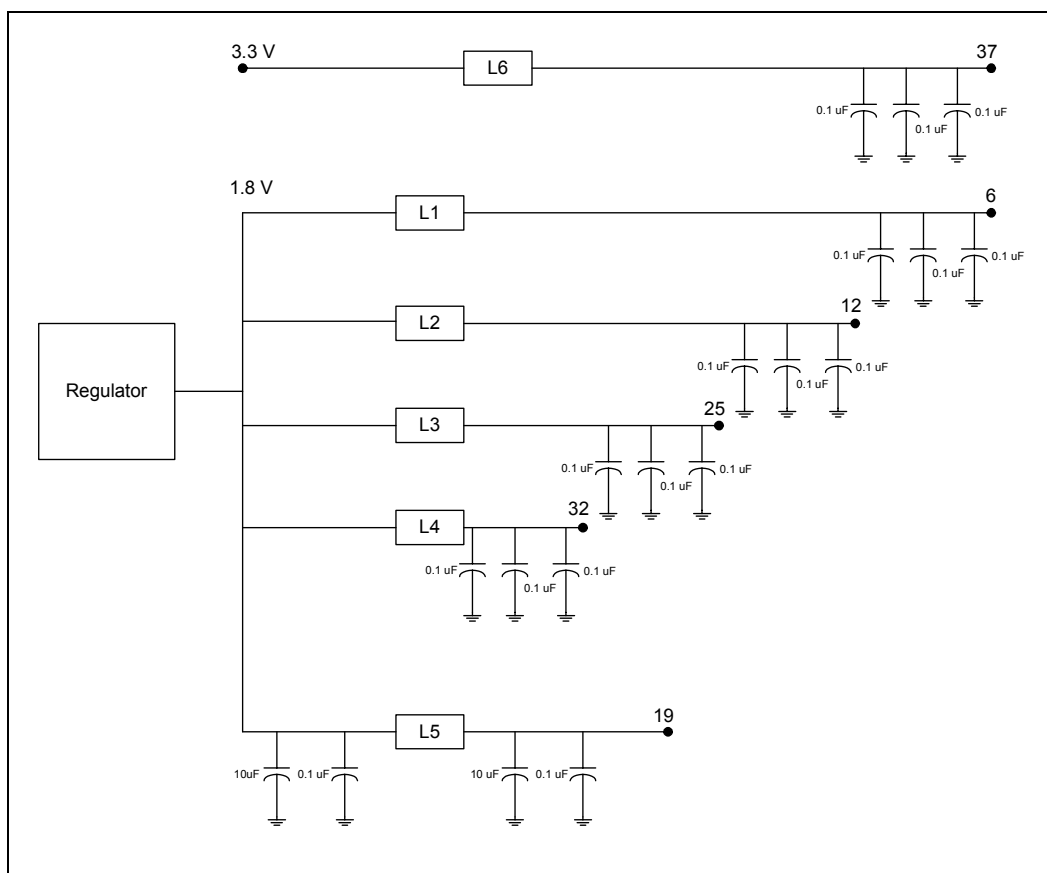


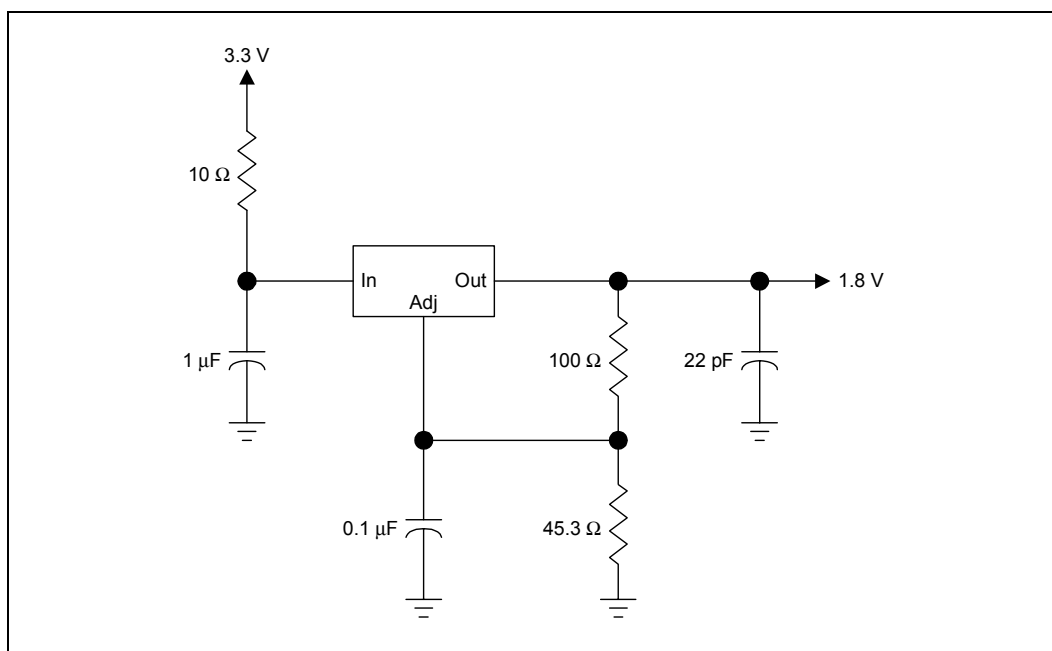
Table 8-5. Ferrite Bead Specifications (L1, L2, L3, L4, L5, L6)

Requirement	Specification
Impedance	>50 Ω at 100 MHz
Series Resistance	< 0.5 Ω
I_{\max}	> 100 mA

8.3.1.5 VREG Implementation

To provide 1.8 V signals to the necessary pins, you must have a well-designed voltage regulator circuit. The recommended circuit contains one 10 Ω resistor, one 100 Ω resistor, and one 45.3 Ω resistor. The circuit should contain a 1 μ F capacitor, a 0.1 μ F capacitor, and one 22 pF capacitor.

Figure 8-12. VREG Implementation



NOTE: The 22 pF capacitor should be placed near the output of the regulator circuit.

8.3.2 SMBus Considerations

The SMBus controller in the Si13112* part is a master device that will contend with the ICH4. To eliminate the contention, it is recommended to disconnect the SMBus signals to the Serial ATA controller. The SMBus signals on the Serial ATA controller are master device/output signals, and therefore the pins can be left floating.

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AGP 8X

9

This chapter contains information for one possible AGP routing and layout solution that is based on the reference platform. Other implementations of AGP routing may be used with proper simulation based on parameters specified in the design guide available at www.agpforum.org.

Refer to [Section 14.6](#) and [Section 15.5](#) for AGP 8X schematic and layout checklists.

[Table 9-1](#) and [Table 9-2](#) show the AGP signal groups and associated strobes.

Note: The AGP supports both 4X and 8X operation.

Table 9-1. Signal Groups

Group	Signals
1	AD[15:0], C#/BE[1:0], ADSTBF0, ADSTBS0
2	AD[31:16], C#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0), ADSTBF1, ADSTBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0), SBSTBF, SBSTBS
4	IRDY, TRDY, FRAME, SERR# (AGP 2.0), SERR (AGP 3.0), STOP, DEVSEL, PAR
5	RBF# (AGP 2.0), RBF (AGP 3.0), WBF# (AGP 2.0), WBF (AGP 3.0), REQ, GNT

Table 9-2. Associated First and Second Strokes

Group	Signals	First Strobe	Second Strobe
1	AD[15:0], C#/BE[1:0]	ADSTBF0	ADSTBS0
2	AD[31:16], C#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0)	ADSTBF1	ADSTBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0)	SBSTBF	SBSTBS

9.1 Recommended AGP 8X Routing Parameters

The AGP 8X signals must be routed directly from the MCH to the AGP connector with all signals referenced to VSS. A consistent VSS reference plane must be maintained at all times. In addition, all signals within an address/data group must be routed on the same layer (see [Table 9-1](#) for address/data groups). [Table 9-3](#) summarizes the routing parameters for the AGP interface.

Table 9-3. AGP 8X Routing Parameters

Signal Group	Trace Impedance (Z_0) ¹	Layer	Spacing	Min Length	Max Length
Strobe to Strobe	60 Ω ¹	Stripline	20 mils	2.5"	7.0"
		Microstrip	25 mils	2.5"	6.0"
Strobe to Data		Stripline	20 mils	2.5"	7.0"
		Microstrip	25 mils	2.5"	6.0"
Data to Data		Stripline	20 mils	2.5"	7.0"
		Microstrip	20 mils	2.5"	6.0"
Common Clock		Stripline	15 mils	2.5"	7.5"
		Microstrip	15 mils	2.5"	7.5"

NOTE:

1. To meet the 60 Ω trace impedance requirement, a trace width of 5 mils was used based on the board stack-up described in [Section 3.2](#). The trace width needed to meet the 60 Ω requirement will vary according to platform stack-up.

9.2 Length Matching

The data groups shown in [Table 9-2](#) must match the strobes within 25 mils. First and second strobes must match to within 5 mils. There are no requirements for length matching between groups, and there are no length matching requirements for signals in groups 4 and 5.

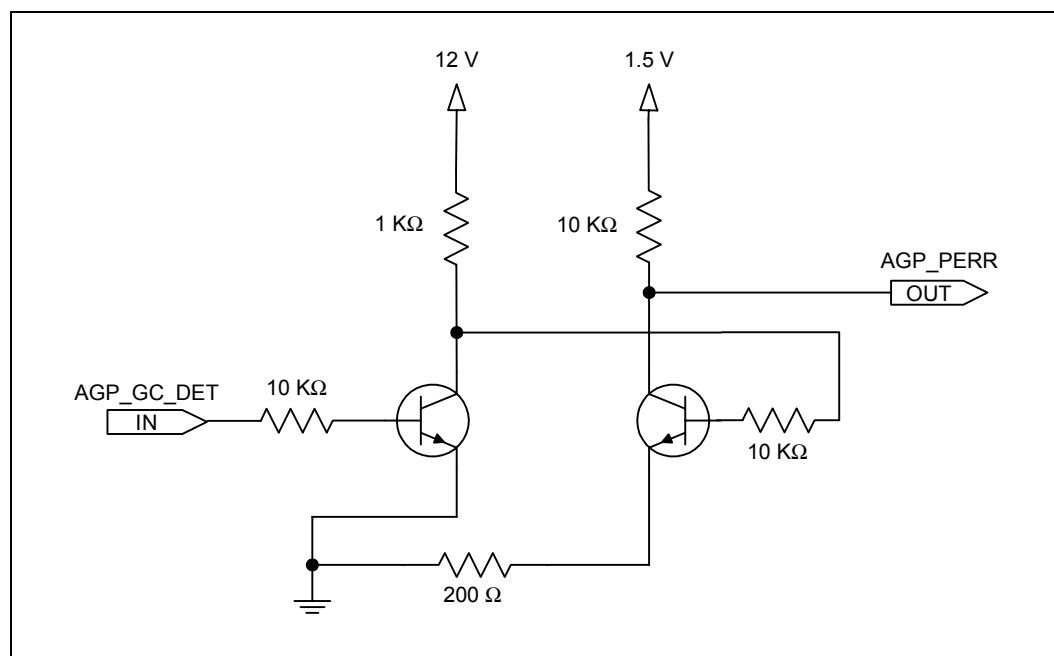
Note: MCH package lengths must be considered when tuning the AGP bus.

9.3 Miscellaneous Signal Requirements

9.3.1 SERR/PERR

The PERR signal is not supported by the MCH and must be supplied to the card based on the GC_8XDET signal. SERR# (AGP2.0) or SERR (AGP 3.0) routes between the connector and the MCH with no special termination. See Figure 9-1 for a PERR reference circuit. The circuit supplies pull-down to ground during 8X operation, and a pull-up to 1.5 V during 4X operation.

Figure 9-1. PERR Reference Circuit



9.3.2 TYPEDET

The TYPEDET signal is not required due to the use of a 1.5 V connector.

9.3.3 PRCOMP_AGP[1:0]

These signals are used to calibrate the AGP buffers. The PRCOMP signals each require a 43 Ω resistor to VCC_AGP.

9.3.4 **PREF_AGP[1:0]**

A complex VREF circuit is required to meet the reference voltage requirements for AGP 4X and 8X. One possible implementation of this circuit can be found in the AGP Design Guide available at www.agpforum.org.

While the VREF voltage for AGP 8X mode is 0.35 V, the circuit implemented in the CRB schematics seems to show a voltage of only 0.3 V. If the resistance across the transistor is taken into account, it can be shown that the circuit generates the required 0.35 V.

9.3.5 **PSWNG_AGP[1:0]**

Provide the reference voltages used by the AGP RCOMP circuits. PSWNG_AGP is based on a resistor divider circuit and comes off of 1.5 V. The voltage level is 0.8 V for 8X mode and is the maximum voltage for the AGP signal bus. For AGP 4X mode, the PSWNG_AGP level is a “don’t care.”

Intel® I/O Controller Hub 4 (ICH4) 10

10.1 System Overview

The ICH4 is designed for a variety of processors/memory controller hubs and has improved enhancements over the Intel® ICH2 and Intel® ICH3.

The ACPI compliant ICH4 platform can support the Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH4 also supports Wake-on-LAN for remote administration and troubleshooting.

The ICH4 integrates an UltraATA/100 controller, one EHCI host controller, and three UHCI host controllers supporting six external ports, LPC interface controller, FWH interface controller, PCI interface controller, AC '97 digital controller, integrated LAN controller, and a hub interface for communication with the MCH. The ICH4 component will provide the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

10.1.1 System Features

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates the following functions:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 1 EHCI USB 2.0 Host Controller and 3 UHCI USB 1.1 Host Controllers (Expanded capabilities for six ports)
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC '97 2.3 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

10.1.2 Bandwidth Summary

Table 10-1 provides a summary of the ICH4 system bandwidth.

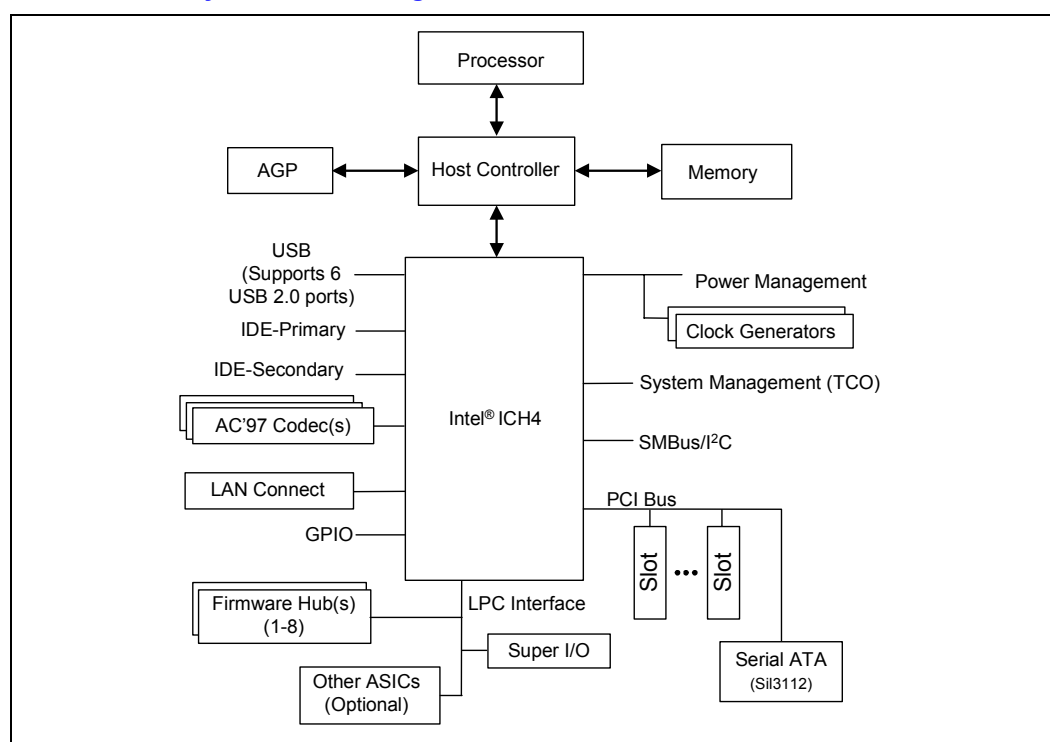
Table 10-1. Intel® ICH4 System Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (bits)	Bandwidth (MB/s)
Hub Interface	66	4	266	8	266
PCI 2.2	33	1	33	32	133
IDE	Up to 44.444 Write Up to 50 Read	1	44.444 (Write) 50 (Read)	16	88.9 (Write) 100 (Read)
LCI	5 – 50	1	5 – 50	3	1.875 – 18.75
AC '97	12.288	1	12.288	1	1.536
LPC	33	1	33	4	16.5
USB 2.0 High Speed	Up to 240 (embedded in data)	Up to 2	480	1	60
SMBus	10	1	10	1	1.25

10.1.3 System Configurations

Table 10-1 shows a typical platform configuration using the ICH4 component.

Figure 10-1. Intel® ICH4 System Block Diagram



10.1.4 Intel® ICH4 Conventions and Terminology

Table 10-2 defines the conventions and terminology that are used in the following ICH4 descriptions.

Table 10-2. Intel® ICH4 Conventions and Terminology

Term	Definition
AC	Audio Codec
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
BER	Bit Error Rate.
CMC	Common Mode Choke.
CNR	Communications and Networking Riser.
EMI	Electro Magnetic Interference.
ESD	Electro Static Discharge.
FS	Full Speed; Refers to USB 1.1 Full Speed.
FWH	Firmware Hub. A nonvolatile memory device used to store the system BOIS.
HS	High Speed. Refers to USB 1.1 High Speed.
Intel® ICH4	I/O Controller Hub Fourth Generation.
LOM	LAN on Motherboard.
LPC	Low Pin Count.
LS	Low Speed. Refers to USB 1.1 Low Speed.
MC	Modem Codec.
PCM	Pulse Code Modulation.
PLC	Platform LAN Connect.
RTC	Real Time Clock.
SMBus	System Management Bus. A two-wire interface through which various system components can communicate.
SPD	Serial Presence Detect.
S/PDIF	Sony/Phillips Digital Interface.
STD	Suspend to Disk.
STR	Suspend to RAM.
TCO	Total Cost of Ownership.
TDM	Time Division Multiplexed.
TDR	Time Domain Reflectometry.
µBGA* CSP	Micro Ball Grid Array.
USB	Universal Serial Bus.

10.2 Platform Initiatives

10.2.1 Integrated LAN Controller

The ICH4 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers CPU utilization by off-loading communication tasks from the CPU.

The ICH4 supports several components, depending upon the target market. Available LAN components include the Intel® 82562ET/82562EZ for basic Ethernet 10/100 connection, the Intel® 82562EM/82562EX component which provides an Ethernet 10/100 connection with the added manageability capabilities, the Intel® 82540EM Gigabit Ethernet Controller, and the Intel® 82551QM Fast Ethernet Controller.

Table 10-3. LAN Component Overview

LAN Component	Interface To Intel® ICH4	Connection	Features
Intel® 82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 Pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

10.2.2 Ultra ATA/100 Support

The ICH4 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, and multiword PIO modes for transfers up to 100 MB/sec.

10.2.3 Expanded USB Support

The ICH4 contains three UHCI Host Controllers and one EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of six legacy USB ports. The EHCI Host Controller includes a root hub that supports up to six USB 2.0 ports. The ICH4 supports a maximum of six USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and dependent on the USB device capability, meaning that all ports support HS/FS/LS.

10.2.4 Manageability and Other Enhancements

The ICH4 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

10.2.4.1 SMBus 2.0

The ICH4 integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, PCI cards, etc. The slave interface allows an external microcontroller to access system resources.

The ICH4 platform integrates several functions designed to expand the capability of interfacing several components to the system.

10.2.4.2 Interrupt Controller

The interrupt capabilities of the ICH4 platform maintain the support for up to eight PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH4 supports system bus interrupt delivery.

10.2.4.3 Intel® Compatible Firmware Hub (FWH)

The ICH4 platform supports the Intel Compatible Firmware Hub BIOS Memory size up to 8 MB for increased system flexibility.

10.2.5 AC '97 6-Channel Support

The *Audio Codec '97 (AC'97) Specification, Version 2.3* defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), and/or an audio/modem codec (AMC) in various configurations. The AC '97 specification defines the interface between the system logic and the audio or modem codec known as the “AC-link.”

The ICH4 platform's AC '97 (with the appropriate codecs) improves overall platform integration by incorporating the AC-link. By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the ICH4 platform. In addition, an AC '97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The ICH4 integrated digital link allows several external codecs to be connected to the ICH4. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 10-2). The digital link is expanded to support three audio codecs or a combination two audio codecs and a modem codec (Figure 10-3 and Figure 10-4).

The digital link in the ICH4 is AC '97 compliant, supporting up to three codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

The ICH4 expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Sub Woofer for a complete surround sound effect. ICH4 has expanded support for three audio codecs on the AC-link.

Figure 10-2. AC '97 with Audio/Modem Codec

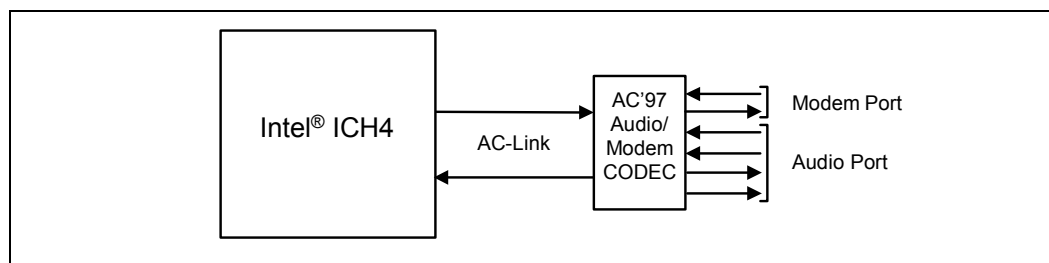


Figure 10-3. AC '97 with Audio Codecs (4 Channel Secondary)

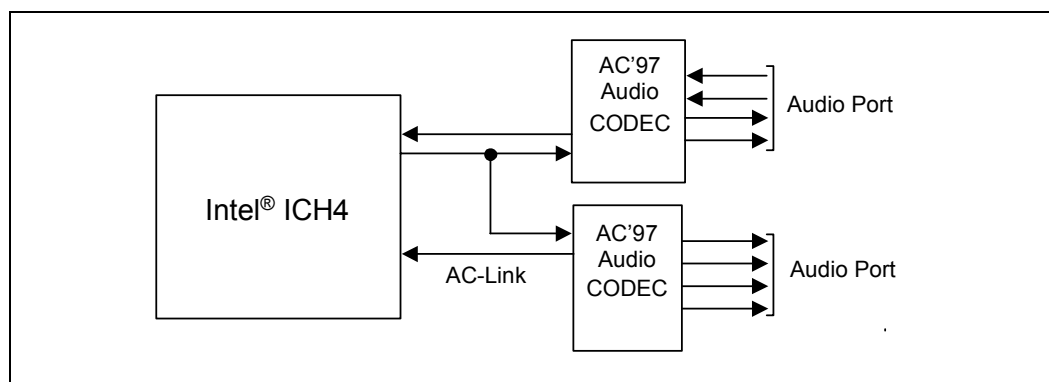


Figure 10-4. AC '97 with Audio and Modem Codec

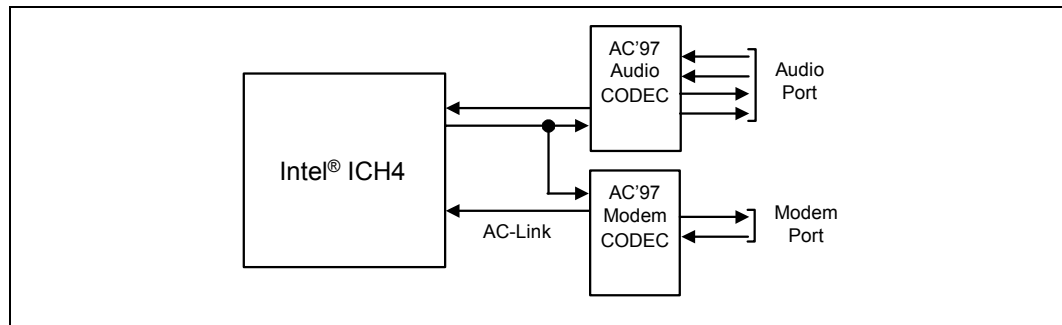
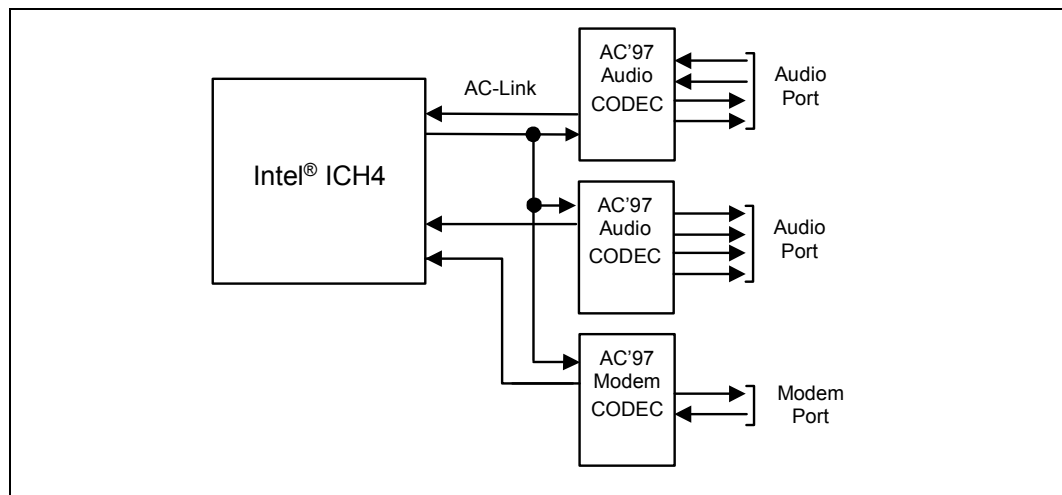


Figure 10-5. AC '97 with 2 Audio and a Modem Codec (4 Channel Secondary)



10.3 Layout/Routing Guidelines

This section describes motherboard layout and routing guidelines for ICH4 based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Warning: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.

Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely.

Warning: Any deviation from these guidelines must be simulated!

10.3.1 General Recommendations

The trace impedance typically noted (i.e., $60\ \Omega \pm 15\%$) is the “nominal” trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

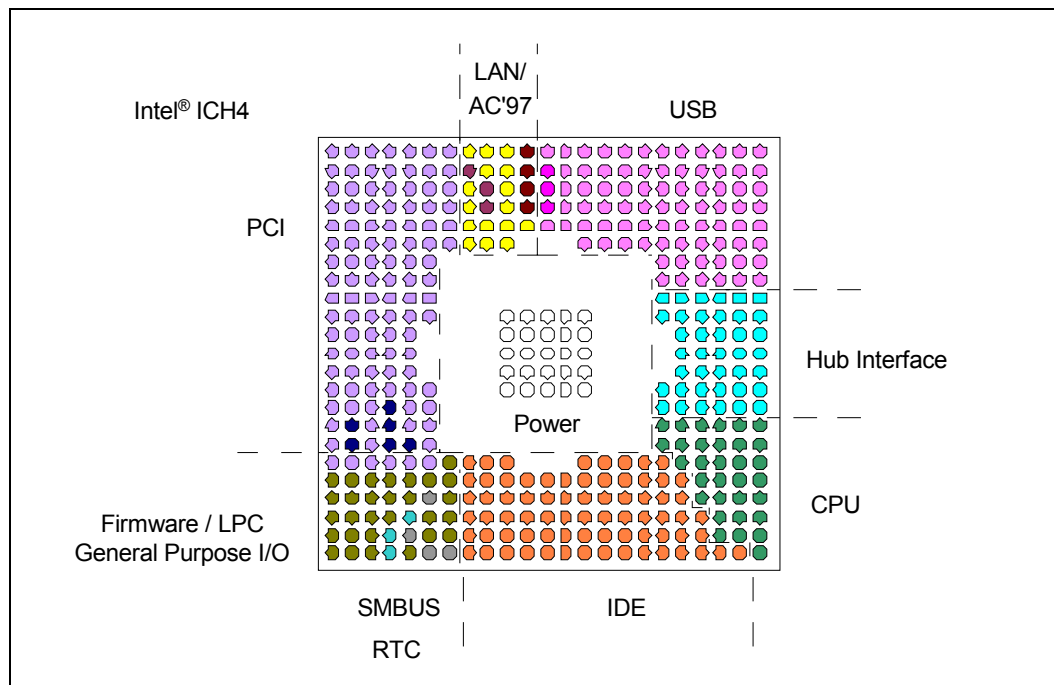
All recommendations in this section (except where noted) assume 5-mil wide traces. If trace width is greater than 5 mils, the trace spacing requirements must be adjusted accordingly (linearly).

If the six layer stack-up is not used, extremely thorough simulations of all interfaces must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

10.3.2 Component Quadrant Layout

The quadrant layouts shown are approximate, and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 10-6. Intel® ICH4 Component Quadrant Layout (Top View)



10.3.3 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options for later use.

The IDE interface can be routed with 5-mil traces on 7-mil spaces and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

Table 10-4. IDE Routing Summary

Trace Impedance	Maximum Trace Lengths	IDE Signal Length Matchin
51 Ω – 69 Ω , 60 Ω target	8 inches	No more than 0.5 inches (500 mils) between the shortest data signal and the longest strobe signal

10.3.3.1 Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct, low impedance chassis path between the motherboard ground and hard disk drives.

10.3.4 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE Controller supports PIO, Multi-word (8237 style) DMA, Ultra DMA modes 0 through 5, and Native Mode IDE. Note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification can be obtained from the Small Form Factor Committee.

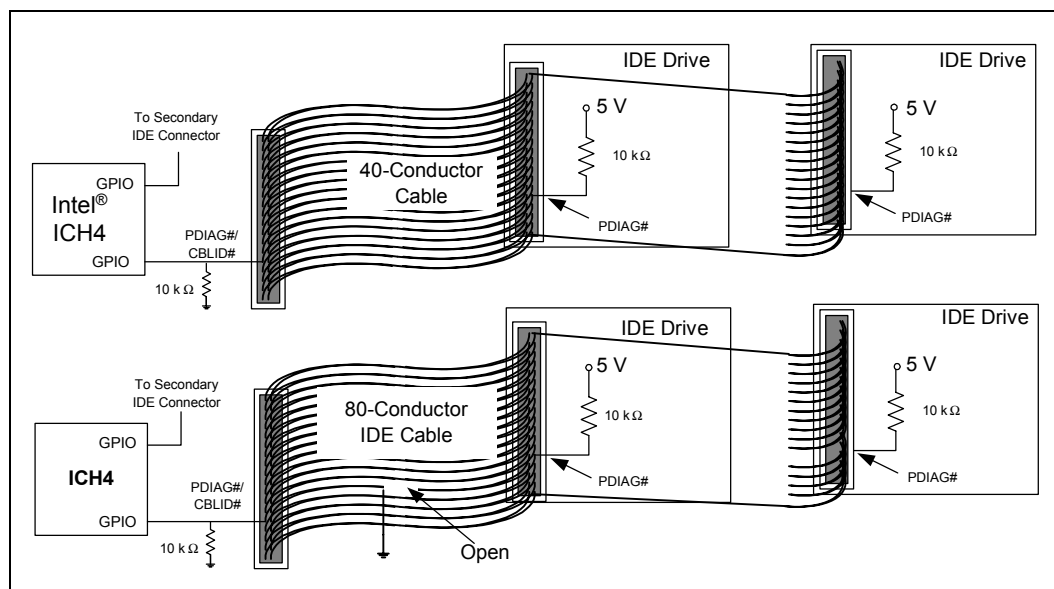
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

10.3.4.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the ATA/ATAPI-6 Standard) requires the use of two GPIO pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 10-7. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 10-7. Combination Host-Side/Device-Side IDE Cable Detection



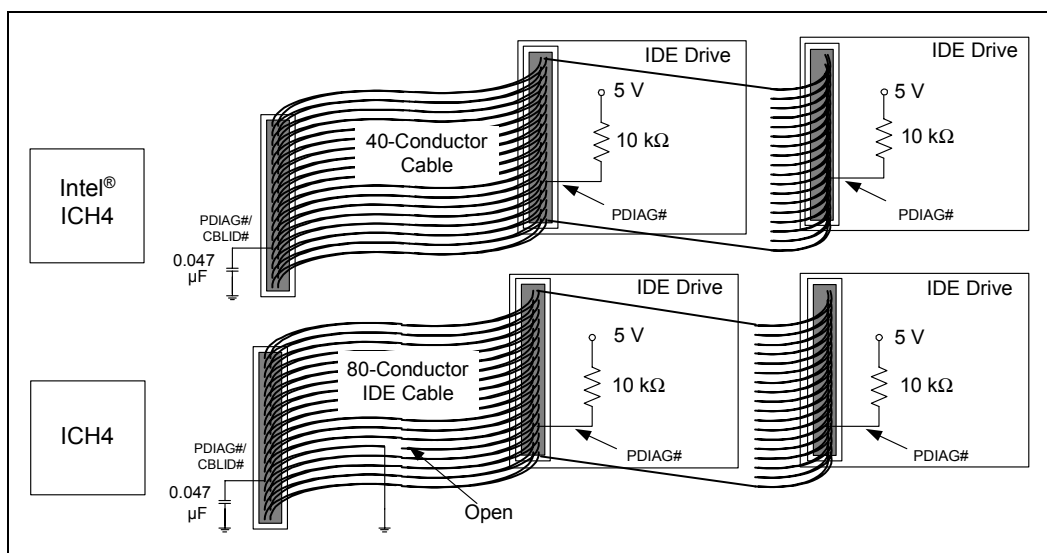
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high there is 40-conductor cable in the system and Ultra DMA modes greater than 2 (Ultra ATA/33) must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-6 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93 bit 13 is 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and should notify the user of the problem.

10.3.4.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 μF capacitor is required on the motherboard as shown in Figure 10-8. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described previously. Note that some drives may not support device-side cable detection.

Figure 10-8. Device Side IDE Cable Detection



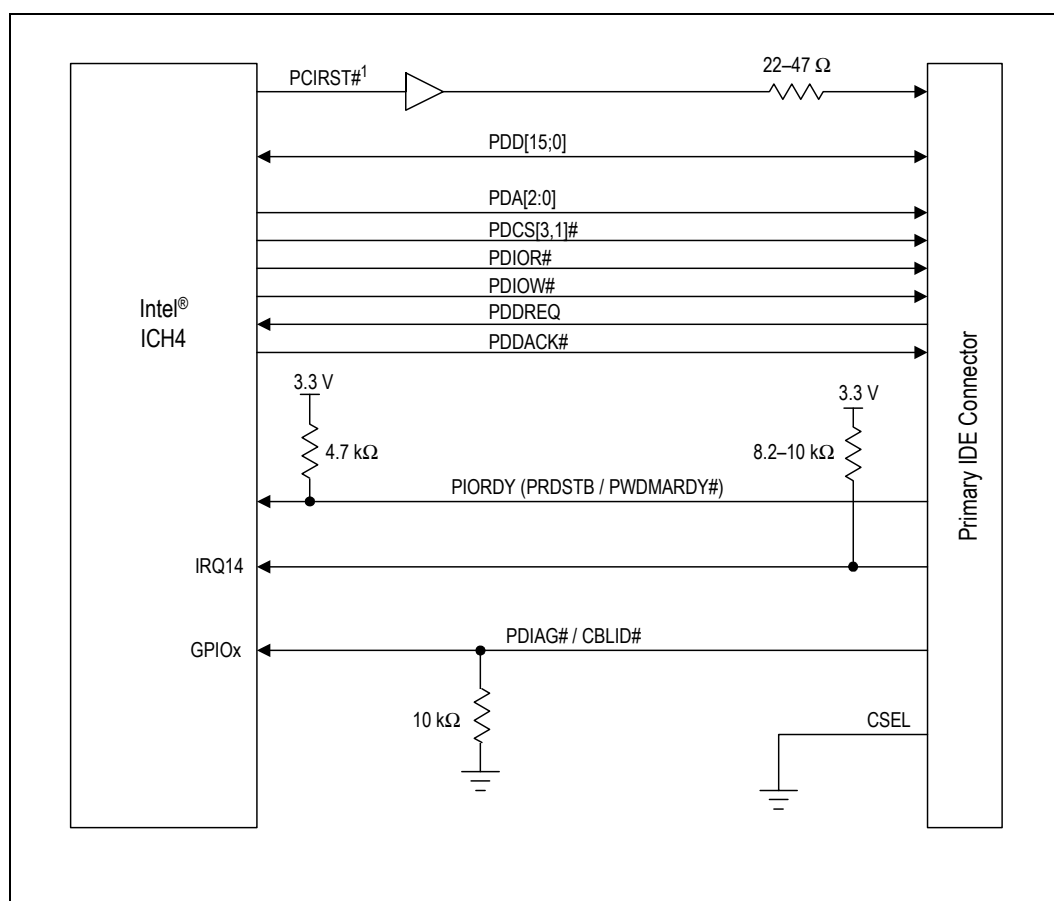
This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 k Ω resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore, the capacitor has no effect. In a 40-conductor cable the signal is connected to the host; therefore, the signal rises more slowly as the capacitor charges. The drive can detect the difference in rise times and reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/ATAPI-4 Standard.

10.3.4.3 Primary IDE Connector Requirements

The requirements for the primary IDE connector are shown in Figure 10-9.

- A 22 Ω – 47 Ω series resistor is required on RESET#. The correct value should be determined for each unique motherboard design based on signal quality.
- An 8.2 k Ω to 10 k Ω pull-up resistor is required on IRQ14 and to VCC3_3.
- A 4.7 k Ω pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 k Ω resistor to ground on the PDIAG#/CBLID# signal is now required on the primary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Figure 10-9. Connection Requirements for Primary IDE Connector



NOTES:

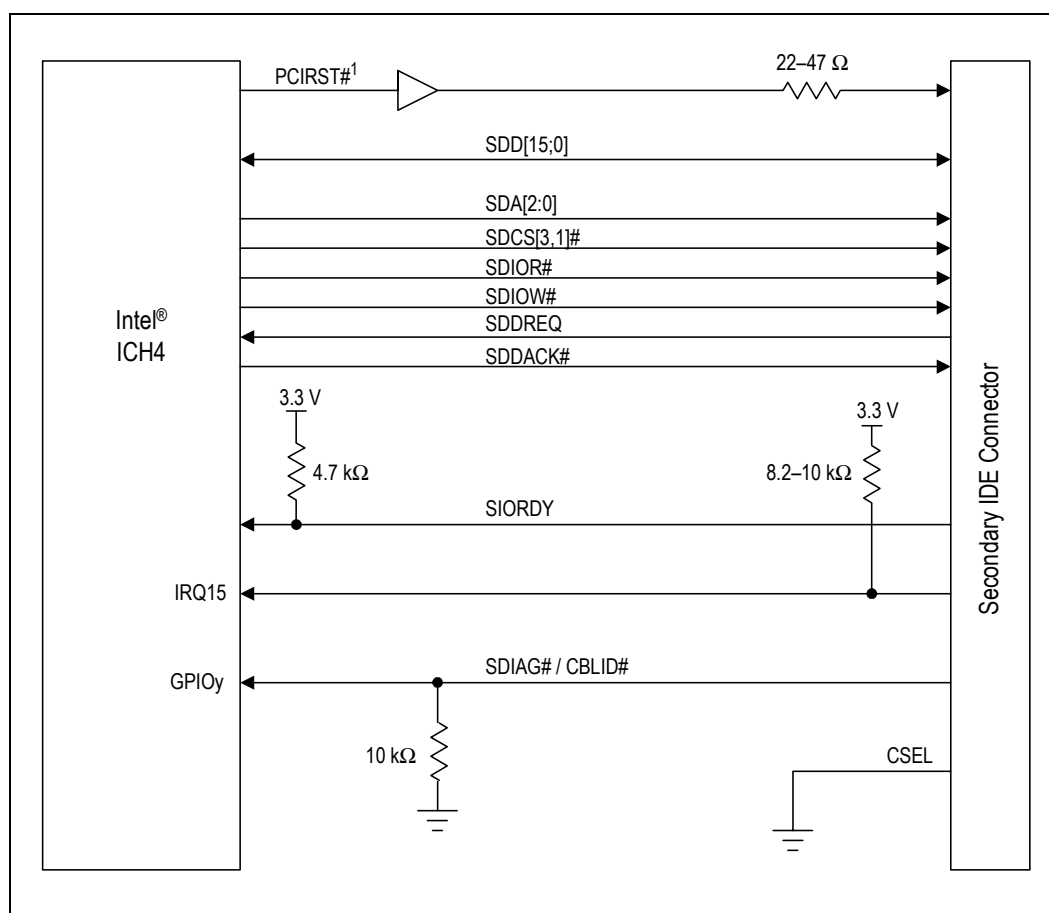
1. Because of ringing, PCIRST# must be buffered.

10.3.4.4 Secondary IDE Connector Requirements

The requirements for the secondary IDE connector are shown in Figure 10-10,

- 22 Ω –47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design based on signal quality.
- An 8.2 k Ω to 10 k Ω pull-up resistor is required on IRQ14 and to VCC3_3.
- A 4.7 k Ω pull-up resistor to VCC3_3 is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 k Ω resistor to ground on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Figure 10-10. Connection Requirements for Secondary IDE Connector



NOTES:

1. Because of ringing, PCIRST# must be buffered.

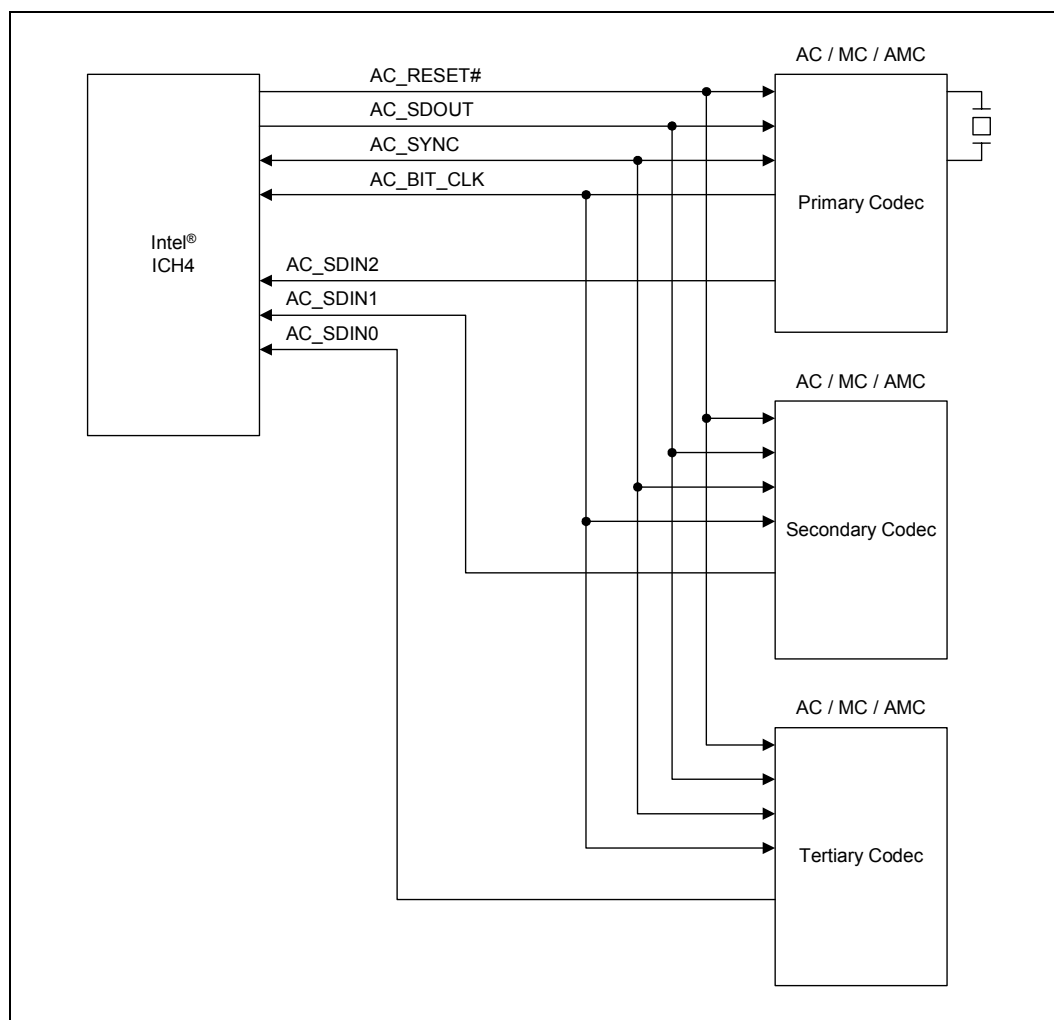
10.3.5 AC '97

The ICH4 implements an AC '97 compliant digital controller. Any codec attached to the ICH4 AC-link must be AC '97 compliant as well. Contact your codec IHV for information on AC '97 compliant products. The *Audio Codec '97 (AC'97) Specification, Version 2.3* is on the Intel website:

<http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec/>

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected. Figure 10-11 shows a three codec ICH4 AC-link topology.

Figure 10-11. Intel® ICH4 AC '97 – Codec Connection



NOTE: If a modem codec is configured as the primary AC-link codec, there should not be any Audio Codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 as described in the ICH4 datasheet.

Using the assumed 6-layer stack-up, the AC '97 interface can be routed using 4-mil traces with 6-mil spacing between the traces. Maximum length between ICH4 to CODEC/CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6 inches for the AC-link. Trace impedance should be $Z_0 = 60 \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4) and to any other codec that is present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK off the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1-S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

The Shut-off bit not set indicates that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 10-12. Intel® ICH4 AC '97 – AC_BIT_CLK Topology

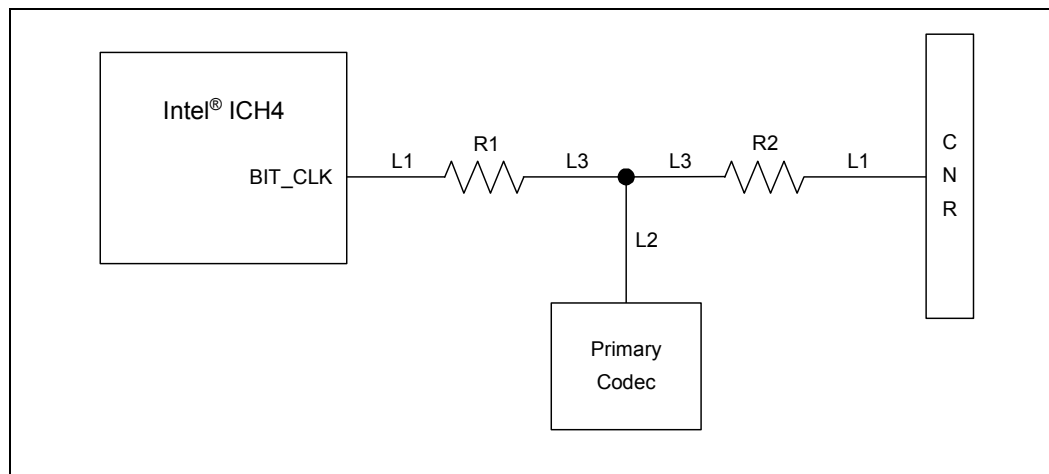


Table 10-5. AC '97 AC_BIT_CLK Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
51 Ω – 69 Ω , 60 Ω target	L1 = (1 to 8) – L3 inches L2 = (0.1 to 6) inches L3 = (0.1 to 0.4) inches L4 = (1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = Optional 0 Ohm resistor for debug purposes	N/A

NOTE: Simulations were performed using Analog Device's codec (AD1885) and the Cirrus Logic's codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.

Figure 10-13. Intel® ICH4 AC '97 – AC_SDOUT/AC_SYNC Topology

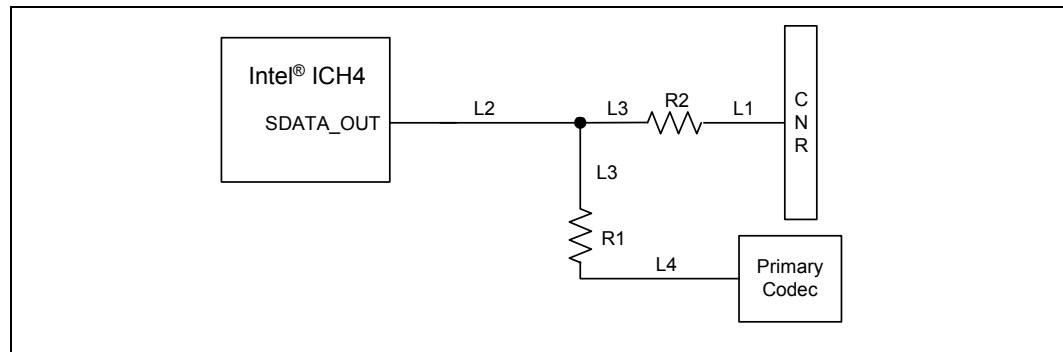


Table 10-6. AC '97 AC_SDOUT/AC_SYNC Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
51 Ω – 69 Ω , 60 Ω target	L1 = (1 to 6) – L3 inches L2 = (1 to 8) inches L3 = (0.1 to 0.4) inches L4 = (0.1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise, R2 = 0 Ohm.	N/A

NOTES:

1. Simulations were performed using Analog Device's* codec (AD1885) and the Cirrus Logic's* codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 10-14. Intel® ICH4 AC '97 – AC_SDIN Topology

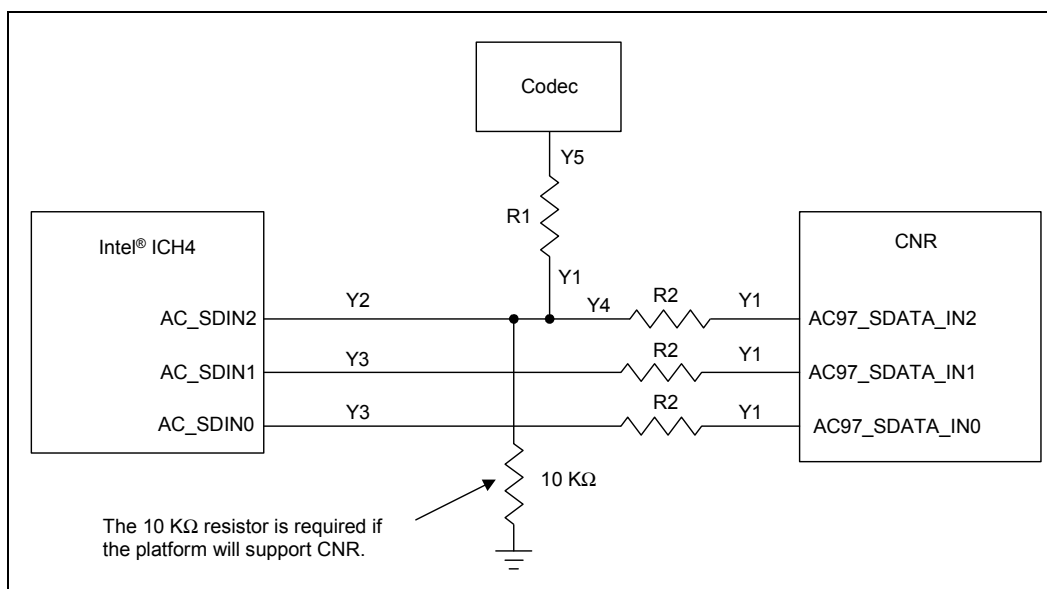


Table 10-7. AC '97 AC_SDIN Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
51 Ω – 69 Ω, 60 Ω target	Y1 = (0.1 to 0.4) inches Y2 = (1 to 8) – Y1 inches Y3 = (1 to 14) – Y1 inches Y4 = (1 to 6) – Y1 inches Y5 = (0.1 to 6) – Y1 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise, R2 = 0 Ohm.	N/A

NOTES:

1. Simulations were performed using Analog Device's* codec (AD1885) and the Cirrus Logic's* codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

10.3.5.1 AC '97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area, and all digital components in another.
- Separate analog and digital ground planes should be provided with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

10.3.5.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC '97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active components such as FET switches, buffers, and logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1–S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. Internal pull-downs will prevent the inputs from floating if no codec is attached to the link, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.3.5.2.1 Valid Codec Configurations

Table 10-8. Valid Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio

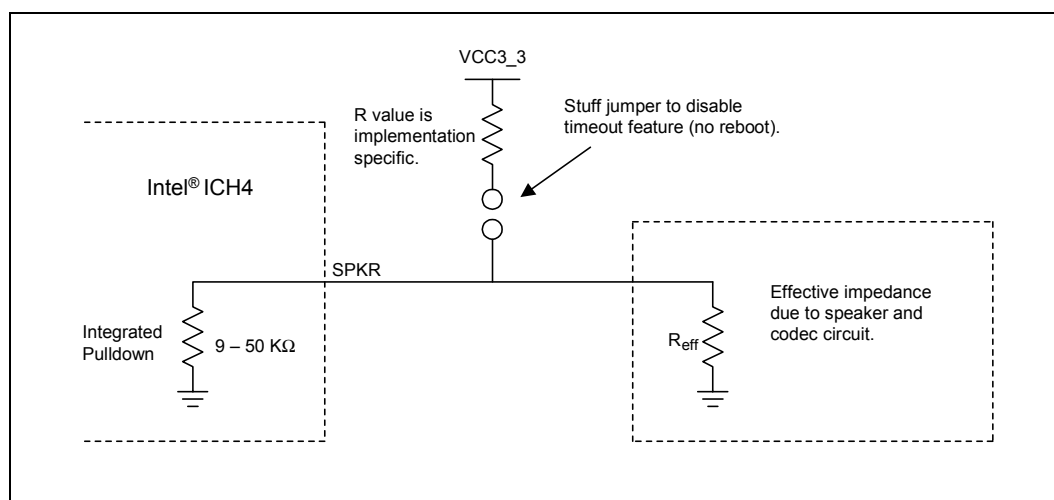
NOTES:

1. For power management reasons, codec power management registers are in audio space. Therefore, if there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system because there is only one set of modem DMA channels.
2. The ICH4 supports a modem codec on any of the AC_SDIN lines. However, the Modem Codec ID must be either 00 or 01.

10.3.5.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker, and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function” based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 10-15). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{EFF}), and the ICH4’s integrated pull-down resistor will be read as logic high ($0.5 V_{CC3_3} + 0.5 V$).

Figure 10-15. Example Speaker Circuit



10.3.6 CNR

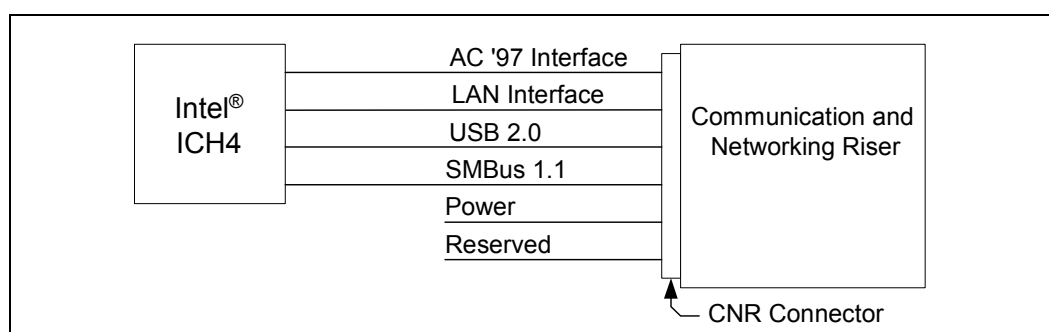
The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, SMBus Interface Power Management Revision 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured before shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Therefore, the system designer will not sacrifice a PCI slot if he decides not to include a CNR in a particular build.

Figure 10-16 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can be either an 82562ET/EZ or an 82562EM/EX component. Refer to the CNR specification for additional information.

For more information, refer to the *Communication Network Riser Specification, Revision 1.2* available at:

<http://developer.intel.com/technology/cnr/download.htm>

Figure 10-16. CNR Interface



10.3.6.1 AC '97 Audio Codec Detect Circuit and Configuration Options

The following are general circuits and guidelines to implement a number of codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2* for Intel's recommended codec configurations.

Table 10-9. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC '97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset) because the CNR codec(s) will be the primary device(s) on the AC '97 Interface
AC97_RESET#	Reset signal from the AC '97 Digital Controller (Intel® ICH4)
SDATA_INn	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH4)

10.3.6.1.1 CNR 1.2 AC '97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.2 AC '97 Disable and Demotion Rules for the motherboard:

1. All AC '97 “non-chaining” codecs on the motherboard **must** always disable themselves when the CDC_DN_ENAB# signal is in a high state.
2. A motherboard AC '97 codec **must** never change its address or SDATA_IN line used, regardless of the state of the CDC_DN_ENAB# signal.
3. On a motherboard containing an AC '97 Controller supporting three AC '97 codecs, the AC '97 v2.2 or AC '97 Revision 2.3 codec on the motherboard **must** be connected to the SDATA_IN2 signal of the CNR connector.
4. A motherboard should not contain any more than a single AC '97 codec.

The above rules allow for forward and backward compatibility between CNR Version 1.1/ 1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification, Revision 1.2*.

Figure 10-17. Motherboard AC '97 CNR Implementation with a Single Codec Down on Board

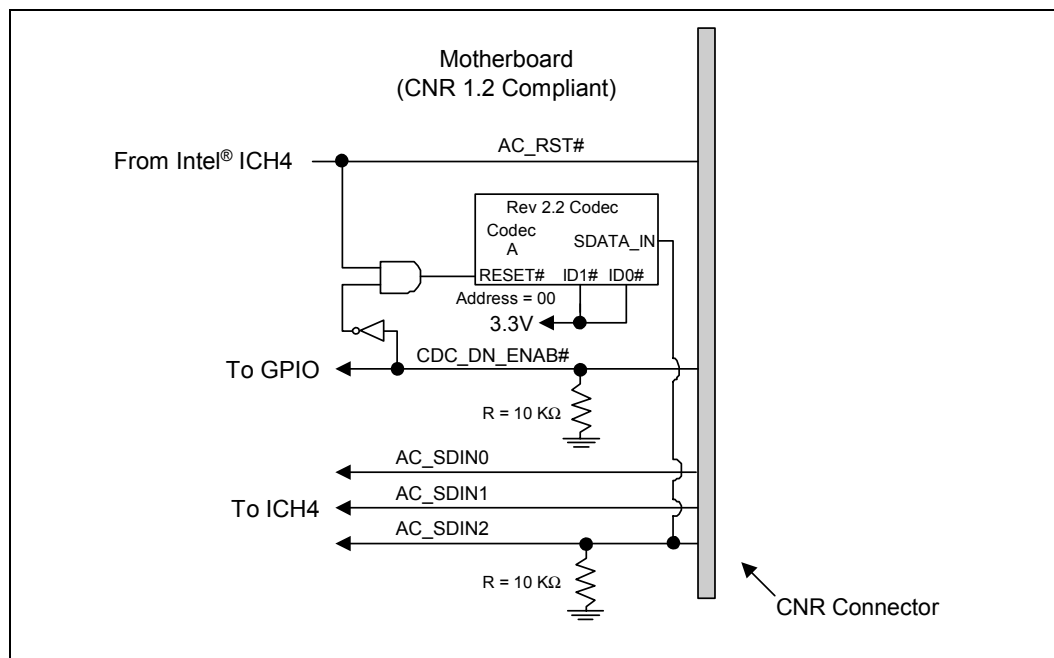
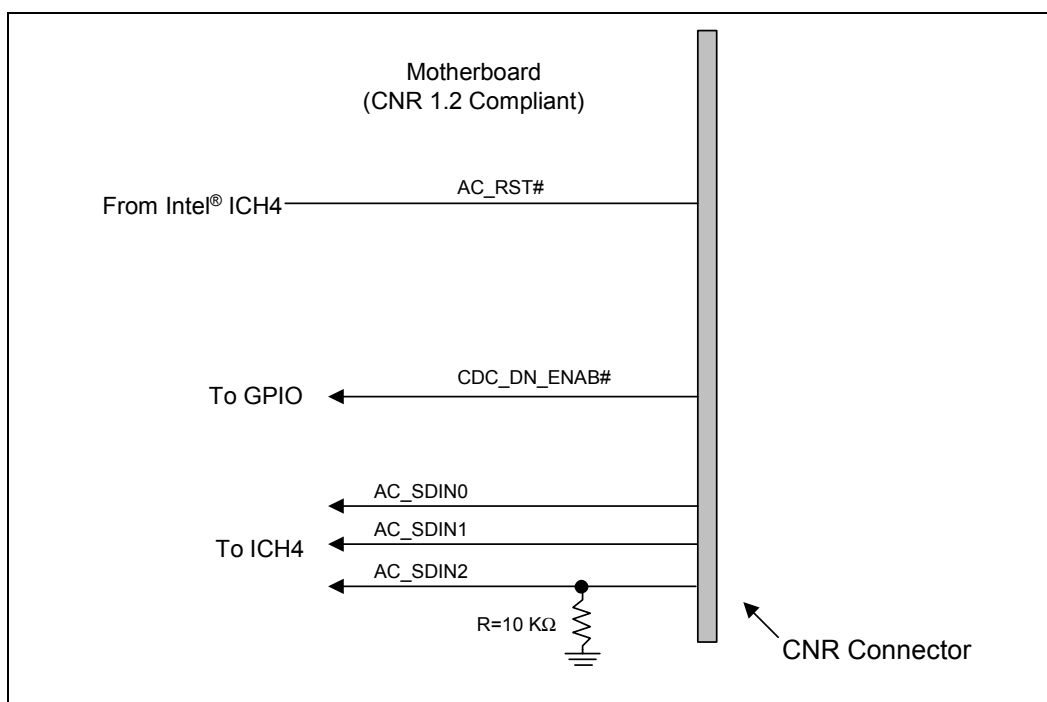


Figure 10-18. Motherboard AC '97 CNR Implementation with no Codec Down on Board

10.3.6.2 CNR Routing Summary

Table 10-10 is a summary of the CNR Riser routing requirements.

Table 10-10. CNR Routing Summary

Trace Impedance	Maximum Trace Length	Signal Length Matching	Signal Referencing
77 Ω – 103 Ω differential, 90 Ω differential target	10"	No more than 150 mils trace mismatch	Ground
51 Ω – 69 Ω , 60 Ω target	AC_BIT_CLK (See Figure 10-12) AC_SDOUT (See Figure 10-13) AC_SDIN (See Figure 10-14)	N/A	Ground
51 Ω – 69 Ω , 60 Ω target	9.5" (See Table 10-21)	Equal to or up to 500 mils shorter than the LAN_CLK trace	Ground

10.3.7 USB 2.0

10.3.7.1 Layout Guidelines

10.3.7.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems

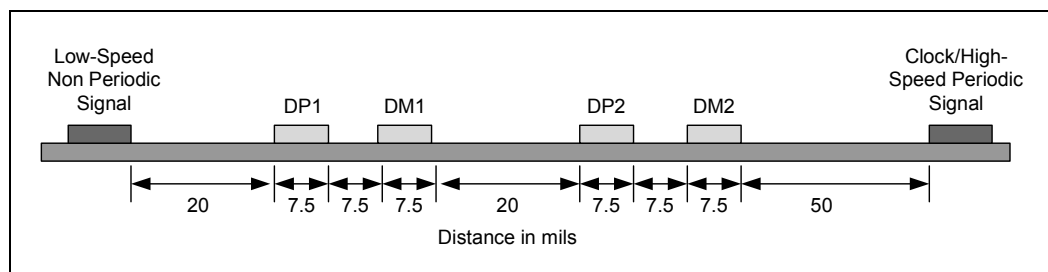
- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, and power connectors).
- USB 2.0 signals should be **ground referenced**.
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90 degrees, use two 45 degree turns or an arc instead of making a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities (see [Figure 10-43](#)).
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Stubs on high-speed USB signals should be avoided because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Similarly, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to [Section 10.3.7.2](#).
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

10.3.7.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 10-19 provides an illustration of the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations will normally occur because of package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 10-19. Recommended USB Trace Spacing



10.3.7.1.3 USBRBIAS/USBRBIAS# Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 $\Omega \pm 1\%$ resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

Figure 10-20. USBRBIAS/USBRBIAS# Connection

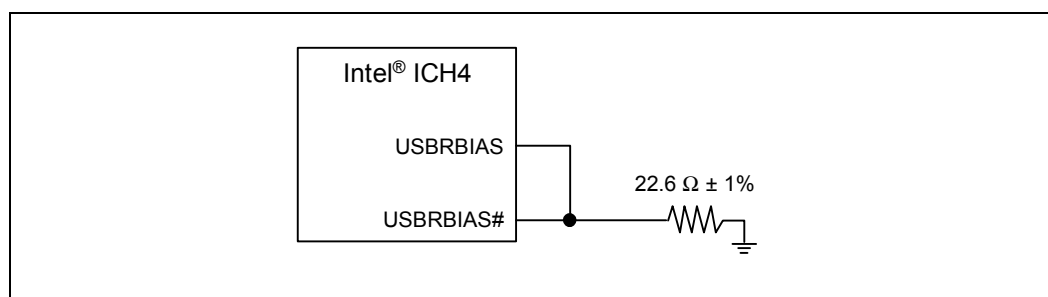


Table 10-11. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	Maximum Trace Length	Signal Length Matching	Signal Referencing
51 Ω – 69 Ω , 60 Ω target	500 mils	N/A	N/A

10.3.7.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See [Section 10.3.7.5](#) for details.

10.3.7.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater than 150 mils.

10.3.7.1.6 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 10-12. USB 2.0 Trace Length Guidelines

USB 2.0 Trace Impedance	Config	Signal Ref	Signal Matching	Motherboard Trace Length		Card Trace Length	Maximum Total Length	
77 Ω – 103 Ω differential, 90 Ω differential target	Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches		N/A	17 inches	
77 Ω – 103 Ω differential, 90 Ω differential target	CNR			8 inches		6 inches	14 inches	
77 Ω – 103 Ω differential, 90 Ω differential target	Front Panel			Cable Lengths		Motherboard Trace Length	Daughter Card Trace Length	Maximum Total Length
				9		6	2	17
				10.5		5	2	17.5
		12		4	2	18		
		13.5		3	2	18.5		
15		2	2	19				

NOTES:

- These lengths are based on simulation results and may be updated in the future.
- All lengths are based upon using a common-mode choke (see [Section 10.3.7.5.1](#) for details on common-mode choke).
- The numbers in [Table 10-12](#) are based on the following simulation assumptions:
 - CNR configuration: max 6 inches trace on add-on card.
 - An approximate 1:1 trade-off can be assumed for Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
- Routing guidelines are based on the stack-up assumptions in [Chapter 3](#).
- Numbers in [Table 10-12](#) are based on the following simulation assumptions:
 - Trace length on front panel connector card assumed a max of 2 inches.
 - USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
- For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

10.3.7.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

10.3.7.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

1. Traces should not cross anti-etch because it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals within 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching capacitors can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 μ F or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching capacitor placed near any high-speed signal crossing. One side of the capacitor should tie to VCC5, and the other side should tie to VCC3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

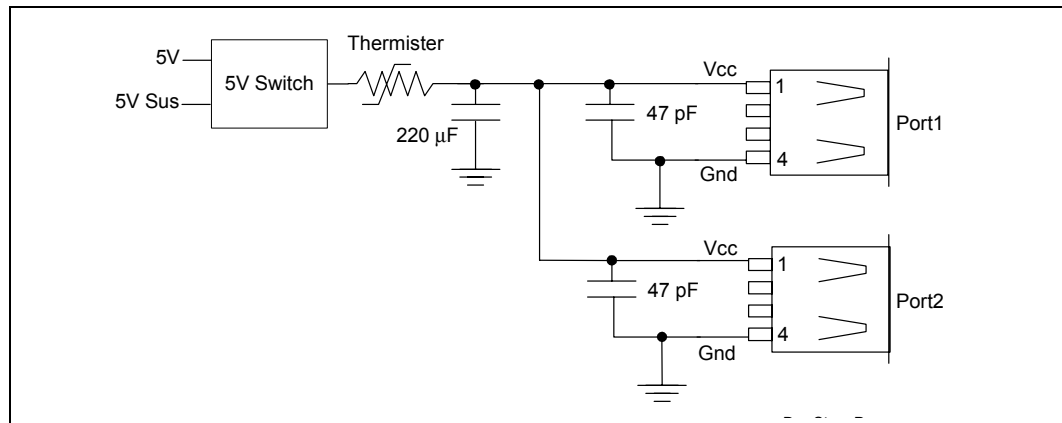
10.3.7.3 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.3.7.4 USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two situations require both bulk capacitance (droop), and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane.

Figure 10-21. Good Downstream Power Connection



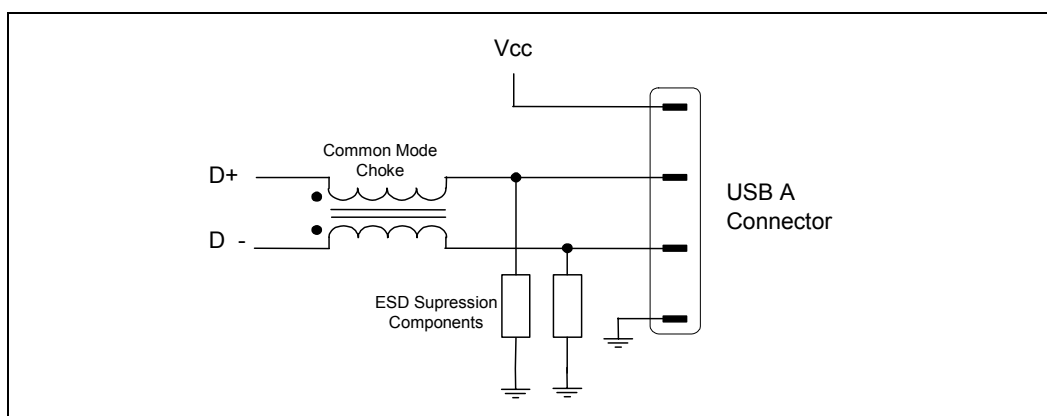
10.3.7.5 EMI Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

10.3.7.5.1 Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card. See [Section 10.3.7.7.3](#)

Figure 10-22. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common Mode Chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results, test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

10.3.7.6 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 because of the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in [Figure 10-22](#). Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

10.3.7.7 Front Panel Solutions

10.3.7.7.1 Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for High/Full-speed cabling for each port with the exceptions described in Cable Option 2. For more information refer to the FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Internal Cable Option 1

Use standard High-speed/Full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *USB 2.0 Specification* with the following additions/exceptions.

- They can share a common jacket, shield, and drain wire.
- Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:
 - The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
 - Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 Specification* that has less than or equal to ½ the resistance of either of the two wires being combined. The data is provided for reference in the following table.

Table 10-13. Conductor Resistance (Table 6-6 from USB 2.0 Specification)

American Wire Gauge (AWG)	Ohm / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: 2–24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See section 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended because of unpredictable impedance characteristics.

10.3.7.7.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the USB 2.0 Specification.

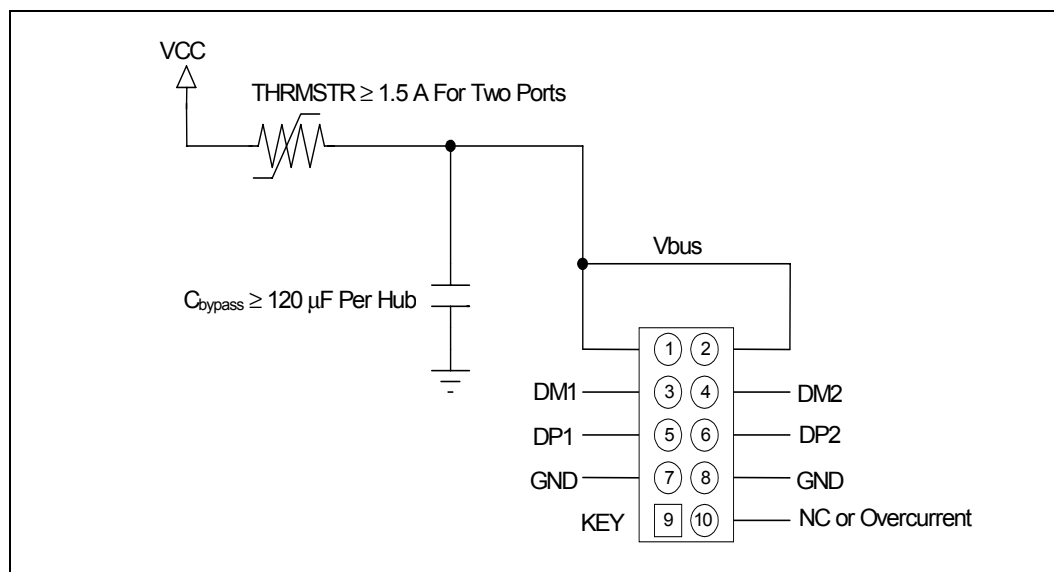
Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in [Table 10-14](#) and the schematic shown in [Figure 10-23](#).

Table 10-14. Front Panel Header Pinout

Pin	Description
1	VCC
2	VCC
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense

Figure 10-23. Front Panel Header Schematic



It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

Routing Considerations

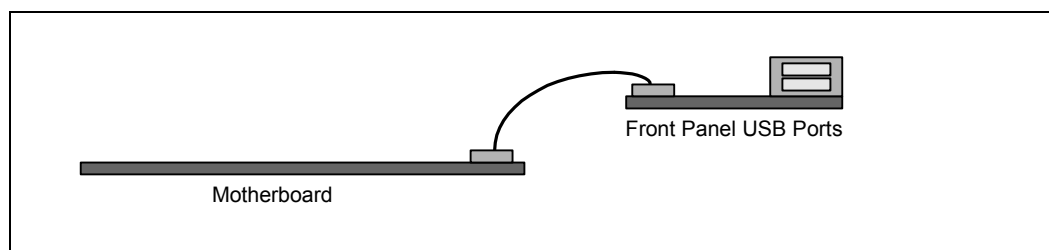
- Traces or surface shapes from VCC to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

10.3.7.7.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 10-24 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information, refer to the FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf

Figure 10-24. Motherboard Front Panel USB Support



When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard because this will usually cause drop/droop and signal quality degradation or failure.

Front Panel Daughter Card Design Guidelines

- Place the Vbus bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as previously outlined for the motherboard.
- Trace length guidelines are given in Table 10-12.

10.3.8 I/O APIC Design Recommendation

The processor does not support I/O APIC. Follow these recommendations.

- **On the ICH4**
 - Tie APICCLK directly to ground
 - Tie APICD0, APICD1 to ground through a 10 kΩ resistor (Separate pull-downs are required if using XOR chain testing.)
- **On the Processor**
 - Consult processor documentation

10.3.9 SMBus 2.0/SMLink Interface

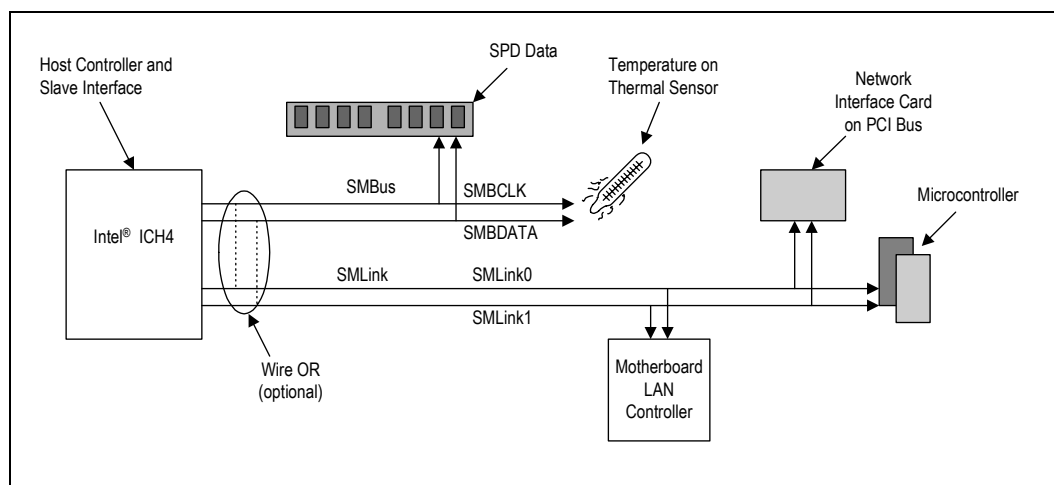
The SMBus interface on the ICH4 uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates a SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals: SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX Platform LAN Connect Component, the ICH4's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals must be tied together externally. This is done by connecting SMLink0 to SMBCLK, and SMLink1 to SMBDATA.

Figure 10-25. SMBUS 2.0/SMLink Interface



NOTE: Intel does not support external access of the ICH4's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4's SMBus Slave Interface by the ICH4's SMBus Host Controller. Refer to the ICH4 datasheet for full functionality descriptions of the SMLink and SMBus interface.

10.3.9.1 SMBus Architecture and Design Considerations

10.3.9.1.1 SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Are there devices that must run in S3?
- Amount of VCC_suspend current available (i.e., minimizing the load of VCC_suspend).

10.3.9.1.2 General Design Issues / Notes

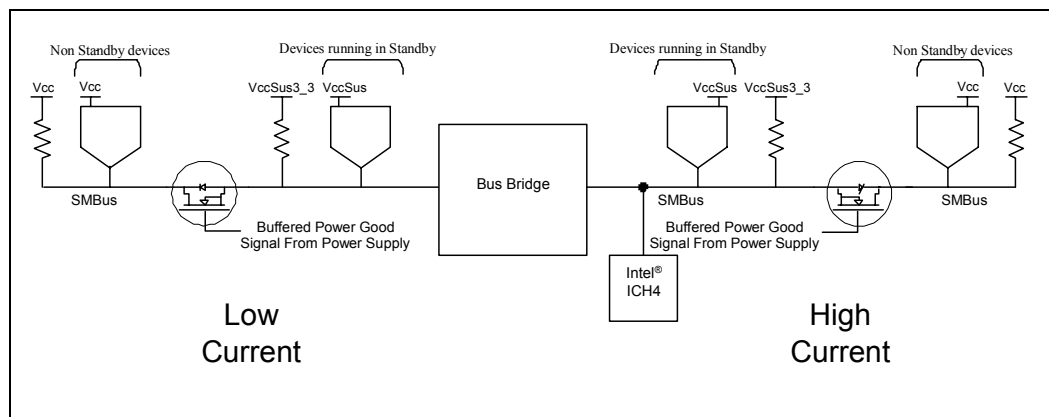
Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally, the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3.
- SMBus devices that can operate in STR must be powered by the VCC_suspend supply.
- If SMBus is connected to PCI, it must be connected to all PCI slots.

10.3.9.1.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices and also allows SMBus devices to communicate while in S3. VCC_suspend leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of an “FET” to isolate the devices powered by the core and suspend supplies (See Figure 10-26).

Figure 10-26. High Power/Low Power Mixed VCC_suspend/VCC Architecture



Added Considerations for Mixed Architecture

- The bus switch must be powered by VCC_suspend.
- Devices that are powered by the VCC_suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.
- The bus bridge can be a device like the Phillips* PCA9515

10.3.9.2 Calculating The Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, a bus bridge device such as the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 10-15. Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® ICH4	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM	28
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length in inches	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96
CNR	1	Pin Capacitance (10 pF) + 6 inch worth of trace capacitance (2 pF/inch) and 2 pF connector capacitance	24

Table 10-16. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For VCC = 3.3 V)
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

10.3.10 PCI

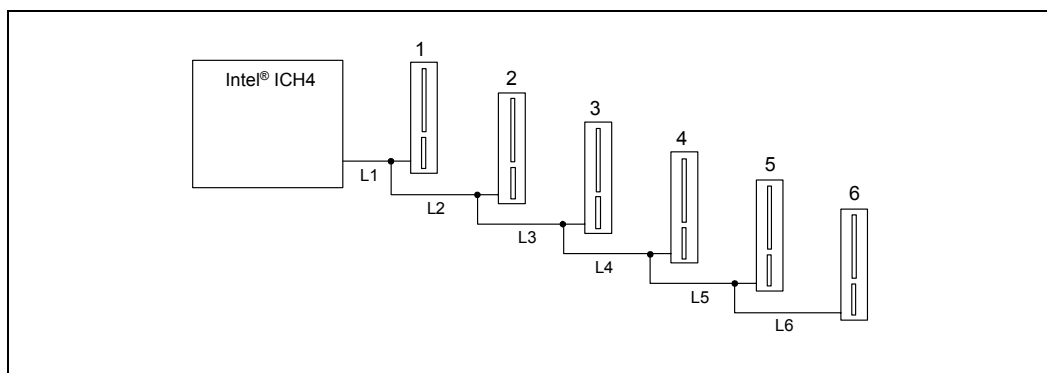
The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4) by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

10.3.10.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the PCI Specification, Revision 2.2 trace length guidelines.

Figure 10-27. PCI Bus Layout Example



NOTE: If a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots. However, it will not take away from the slot functionality.

Figure 10-28. PCI Bus Layout Example with IDSEL

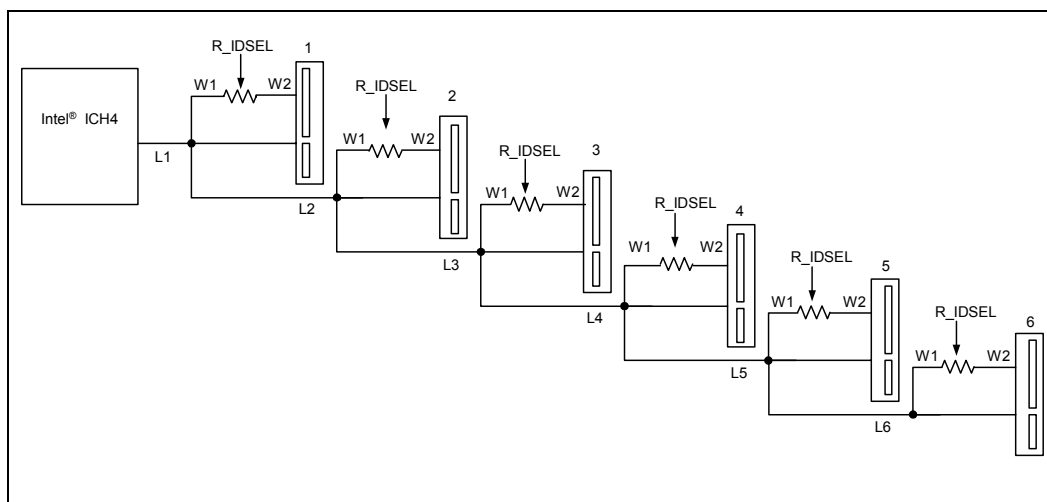


Table 10-17. PCI Data Signals Routing Summary

Trace Impedance	Topology	Maximum Trace Length					
		L1	L2	L3	L4	L5	L6
47 Ω – 69 Ω , 60 Ω target	2 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	N/A	N/A	N/A	N/A
	3 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	1.5 inches	N/A	N/A	N/A
	4 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.0 inches	1.0 inches	1.0 inches	N/A	N/A
51 Ω – 69 Ω , 60 Ω target	5 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 8 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	N/A
	6 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 7 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches

Figure 10-29. PCI Clock Layout Example

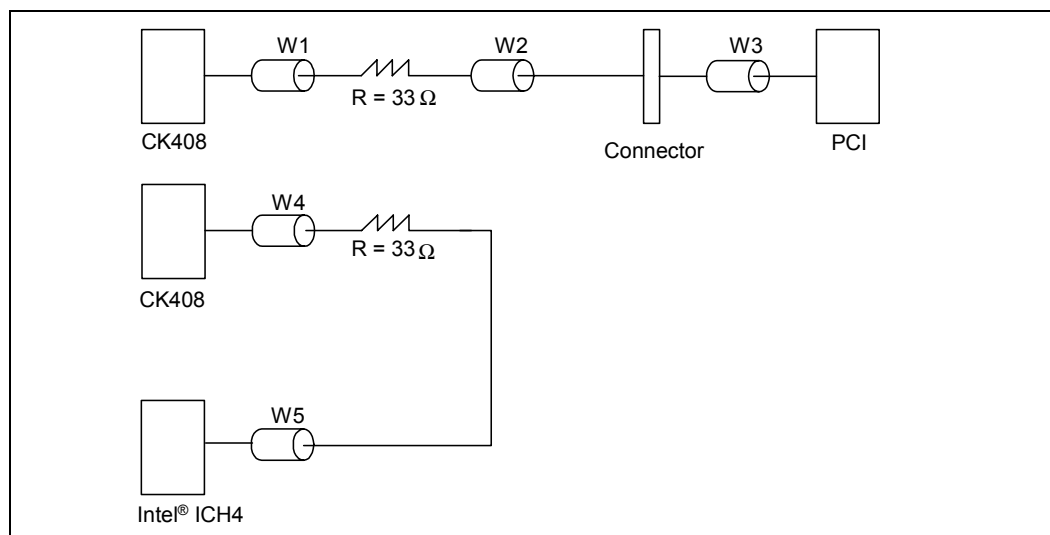


Table 10-18. PCI Clock Signals Routing Summary

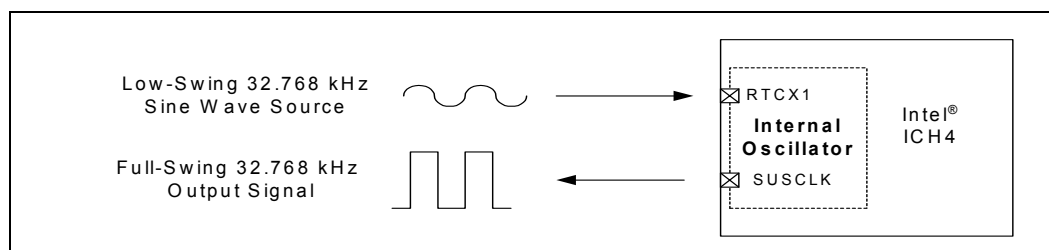
Trace Impedance	Topology	Maximum Trace Length				
		W1	W2	W3	W4	W5
51 Ω – 69 Ω , 60 Ω target	2–6 slots	0.5 inches	(W5 – 4.5) inches	2.5 inches (shown as reference only)	0.5 inches	Can be as long as needed as long as W2 is scaled accordingly

10.3.11 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as to generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK (see Figure 10-30).

Figure 10-30. RTCX1 and SUSCLK Relationship in Intel® ICH4

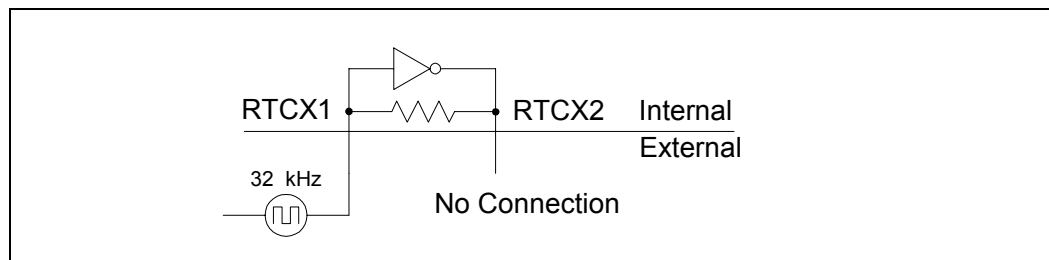


For further information on the RTC, refer to Application Note AP-728 *ICH/ICH4/ICH4-M/ICH3-S/ICH3-M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it's still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated from that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical, a cheap crystal can be used, or a single clock input can be driven into RTCX1 with RTCX2 left as no connect (see Figure 10-31). This is not a validated feature on ICH4.

Note: The peak to peak swing on RTCX1 cannot exceed 1.0 V.

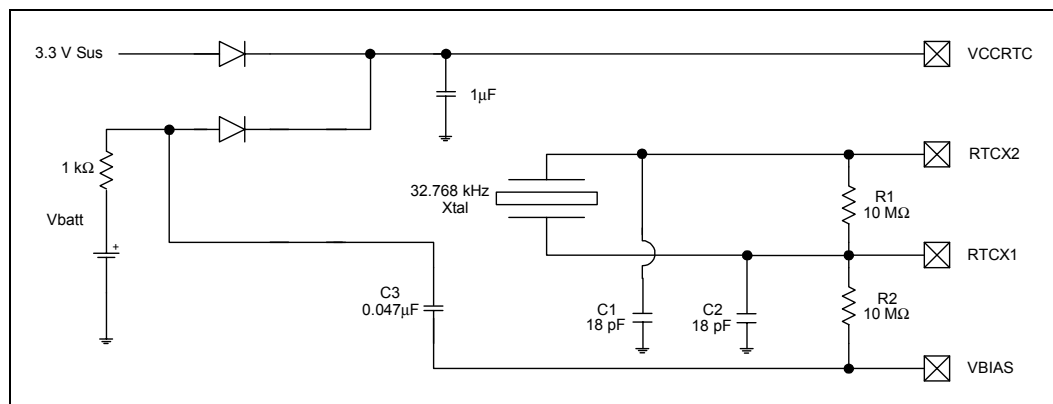
Figure 10-31. External Circuitry for the Intel® ICH4 (Internal RTC Is Not Used)



10.3.11.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 10-32 shows the external circuitry that comprises the ICH4 RTC oscillator.

Figure 10-32. External Circuitry for the Intel® ICH4 RTC



NOTES:

1. The exact capacitor value must be based on the crystal maker's recommendation. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF).
2. VccRTC: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This ball is used to provide a reference voltage. This DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground

Table 10-19. RTC Routing Summary

Trace Impedance	Max Trace Length to Crystal	Signal Length Matching	R1, R1, C1, and C2 Tolerances	Signal Referencing
51 Ω – 69 Ω, 60 Ω target	1 inch	N/A	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.3.11.2 for calculating a specific capacitance value for C1 and C2	Ground

10.3.11.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047 μ F, and capacitor values C₁ and C₂ should be chosen to provide the manufacturer's specified load capacitance (C_{LOAD}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{LOAD} = [(C_1 + C_{IN1} + C_{TRACE1}) * (C_2 + C_{IN2} + C_{TRACE2})] / [(C_1 + C_{IN1} + C_{TRACE1} + C_2 + C_{IN2} + C_{TRACE2})] + C_{PARASITIC}$$

Where:

- C_{LOAD} = crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{IN1}, C_{IN2} = input capacitances at the RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 datasheet.
- C_{TRACE1}, C_{TRACE2} = trace length capacitances measured from Crystal terminals to the RTCX1, RTCX2 pins. These values depend on the characteristics of board material, the width of signal traces, and the length of the traces. Typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

$$C_{TRACE} = \text{trace length} * 2 \text{ pF/inch (assuming a 5 mil trace } \frac{1}{2} \text{ oz. copper)}$$

- C_{PARASITIC} = crystal's parasitic capacitance. This capacitance is created by the exist of 2 electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C₁, C₂ can be chosen such that C₁ = C₂. Using the C_{LOAD} equation, the value of C₁, C₂ can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C₂ can be chosen such that C₂ > C₁. C₁ can then be trimmed to obtain the 32.768 kHz.

In certain conditions, both C₁, C₂ values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C₁, C₂ value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example describes the calculation of practical C₁, C₂ values if theoretical values cannot guarantee the accuracy of the RTC in low temperature conditions:

Example 1

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of C₁ = C₂ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal is –23 ppm (assuming that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C₁, C₂ are chosen to be 6.8 pF instead of 10 pF, The RTC will oscillate at higher frequency at room temperature (+23 ppm), but this configuration of C₁ / C₂ makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C₁ and 2 is the **practical value**.

Note that the temperature dependency of the crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

10.3.11.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during RTC circuit layout and routing. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn pin). Routing the RTC circuit should be kept simple to simplify the trace length measurement and to increase the accuracy of trace capacitance calculations. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be reduced by avoiding routing of adjacent PCI signals close to RTCX1, RTCX1, and VBIAS.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

10.3.11.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

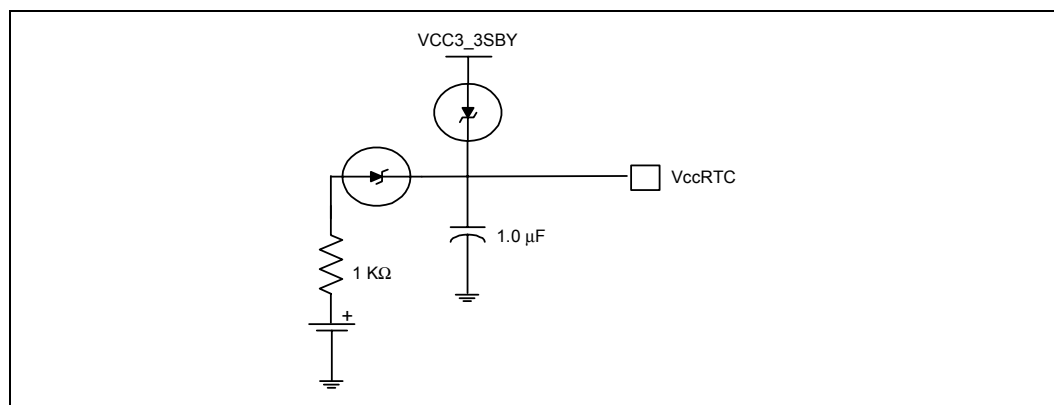
Example batteries are Duracell® 2032, 2025, and 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 μ Ah (assumed usable) and the average current required is 3 μ A, the battery life will be at least:

$$170,000 \mu\text{Ah} / 5\mu\text{A} = 34,000 \text{ h} = 3.9 \text{ years}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

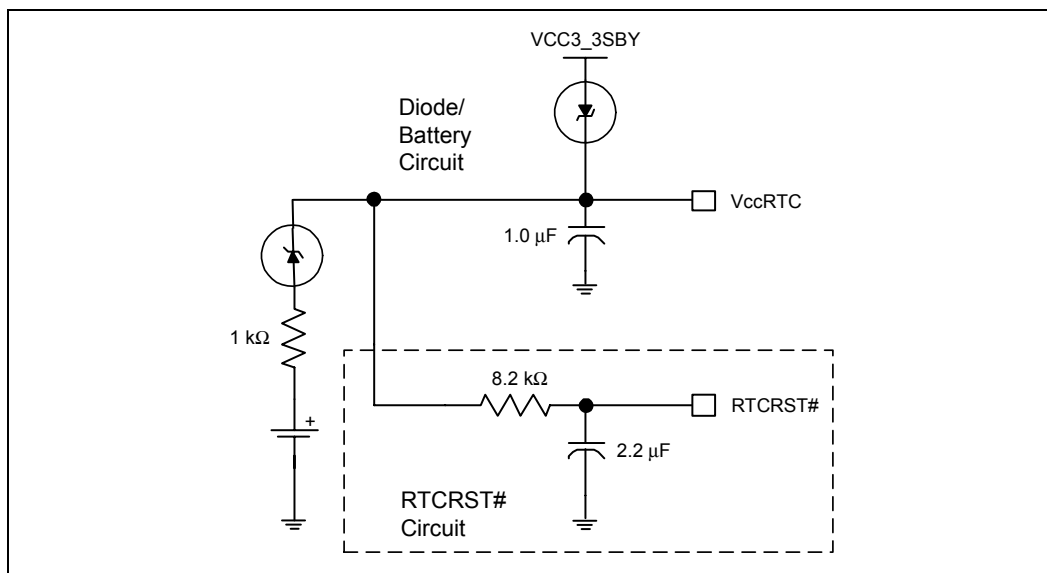
The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. [Figure 10-33](#) is an example of a diode circuit.

Figure 10-33. A Diode Circuit to Connect RTC External Battery



10.3.11.5 RTC External RTCRST# Circuit

Figure 10-34. RTCRST# External Circuit for the Intel® ICH4 RTC



The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms–25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCN_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. Therefore, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in the [Figure 10-33](#)) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. [Figure 10-34](#) is an example of this circuitry that is used in conjunction with the external diode circuit.

10.3.11.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered from the RTC oscillation signal by the RC Network of R2 and C3 (see [Figure 10-32](#)). Therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 filters out most of the AC signal that exists on this ball. However, the noise on this ball should be kept to a minimum to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX and RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details about measuring techniques.

Note: VBIAS is very sensitive to environmental conditions.

10.3.11.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle can be between 30-70%. A SUSCLK duty cycle beyond the 30-70% range indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe), and is an appropriated signal that is used to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

10.3.11.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VccRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in [Figure 10-34](#), meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.3.12 Internal LAN Layout Guidelines

The ICH4 provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, 82562EZ/82562ET and 82562EX/82562EM Platform LAN Connect components.

Table 10-20. LAN Component Connections/Features

LAN Component	Interface To Intel® ICH4	Connection	Features
Intel® 82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN* (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 Pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

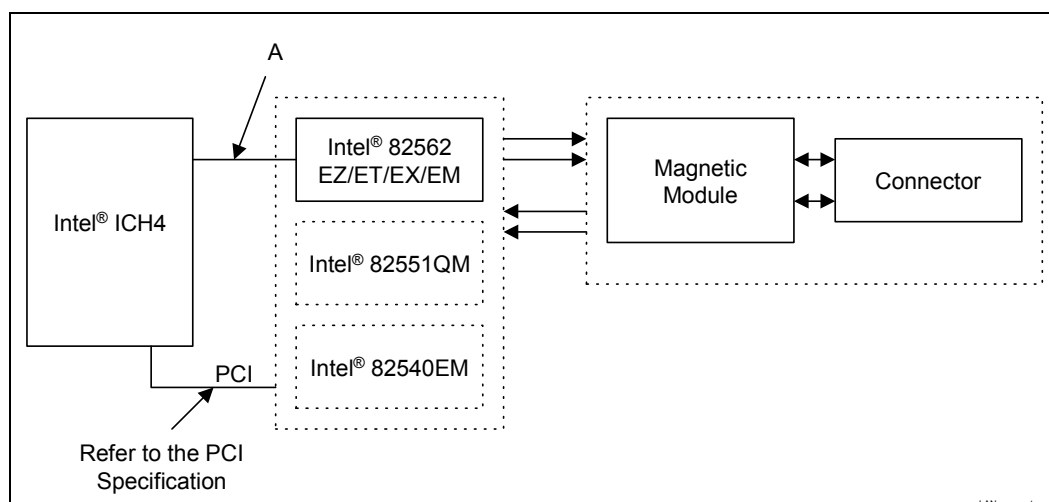
Which LAN component to use on the ICH4 platform depends on the end user's need for connection speed, manageability, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

10.3.12.1 Footprint Compatibility

The 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, and the 82562EX/82562EZ Platform LAN Connect devices are all manufactured in a footprint-compatible 15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the use of some pins on the 82540EM differ from the use on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as “pin compatible.” The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design.

Design guidelines are provided for each required interface and connection. Refer to the following figures and tables for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and the 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 10-35. Intel® ICH4/Platform LAN Connect Sections



NOTE: 82562EZ/EX, 82551QM, and 82540EM are footprint compatible with each other. 82562ET/EM are footprint compatible with each other.

Table 10-21. LAN Design Guide Section Reference

Layout Section	Figure 10-35 Reference	Design Guide Section
Intel® ICH4 – LAN Connect Interface (LCI)	A	Section 10.3.12.2, “Intel® ICH4 – LAN Connect Interface Guidelines”
Intel® 82562EZ/EX Intel® 82562ET/EM	A	Section 10.3.13, “Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM”

10.3.12.2 Intel® ICH4 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562ET and 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

10.3.12.2.1 Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation

LOM (LAN On Motherboard) or CNR Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EM, 82562ET, or CNR are uniquely installed.

Figure 10-36. Single Solution Interconnect

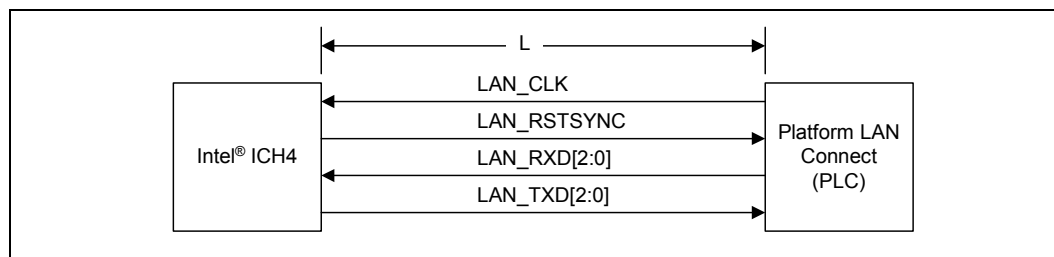


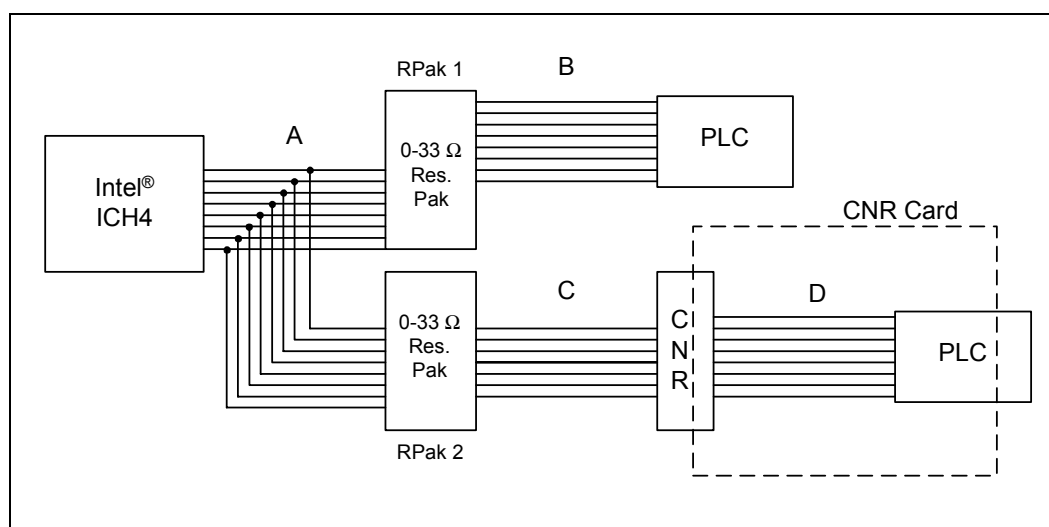
Table 10-22. LAN LOM or CNR Routing Summary

	Maximum Trace Length	Trace Impedance	Signal Referencing	LAN Signal Length Matching
Intel® 82562EZ/ET/EX/EM	4.5 to 12 inches	51 Ω – 69 Ω, 60 Ω target	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/ET/EX/EM on CNR	2 to 9.5 inches			

LOM (Lan On Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time. (See [Figure 10-37](#) and [Table 10-23](#)).

Figure 10-37. LOM/CNR Interconnect



NOTE: Either RPak 1 or RPak 2 can be populated, but not both.

Table 10-23. LAN LOM/CNR 'Dual Routing Summary

	Maximum Trace Length				Trace Impedance	Signal Ref.	LAN Signal Length Matching
	A	B	C	D			
Intel® 82562EZ/ET/EX/EM	0.5 to 7.5 inches	4 to (11.5 – A) inches	NA	NA	51 Ω – 69 Ω, 60 Ω target	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/ET/EX/EM on CNR ¹	0.5 to 7.5 inches	NA	1.5 to (9 – A) inches	0.5 to 3 inches			

NOTES:

1. Total motherboard trace length should not exceed 9 inches

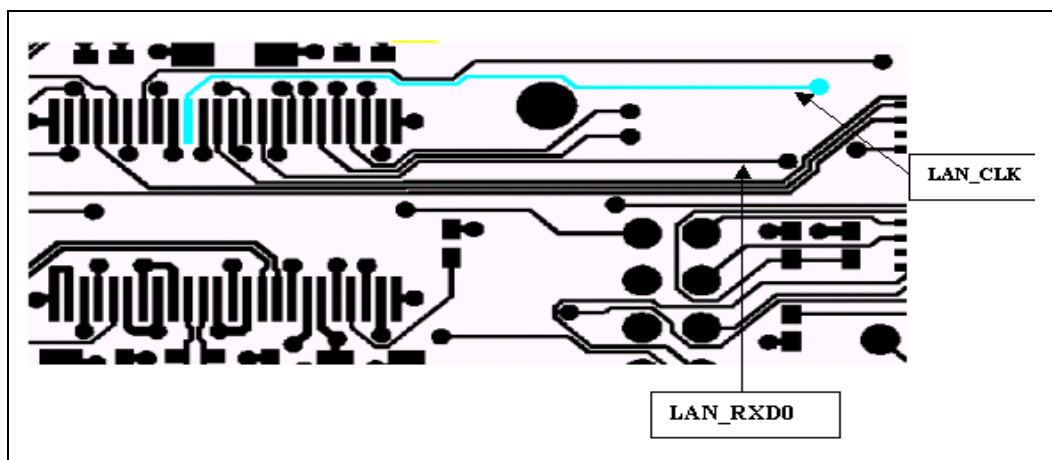
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 to 33 Ω (See [Section 10.3.12.2.5](#)).

10.3.12.2.2 Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace, or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 10-38. LAN_CLK Routing Example



10.3.12.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. tRMATCH is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.3.12.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of $60\ \Omega \pm 15\%$ is strongly recommended; otherwise, signal integrity requirements may be violated.

10.3.12.2.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A $0\ \Omega$ to $33\ \Omega$ series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.3.12.2.6 Disabling Intel® ICH4 Integrated LAN

The LAN Connect Interface on the ICH4 can be left as a no-connect if it is not used.

10.3.13 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM

For correct LAN performance, designers must follow the general guidelines outlined in [Section 10.3.12.2](#). Additional guidelines for implementing an 82562EZ/ET/EX/EM Platform LAN Connect component are provided below.

10.3.13.1 Guidelines for Intel® 82562EZ/ET/EX/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.3.13.1.1 Crystals and Oscillators

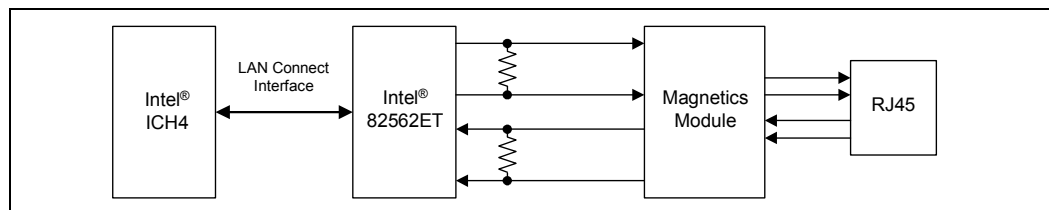
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise-free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM, keeping the trace length as short as possible, and do not route any noisy signals in this area.

10.3.13.1.2 Intel® 82562EZ/EX / Intel® 82551QM Termination Resistors

The $100\ \Omega$ ($\pm 1\%$) resistor that is used to terminate the differential transmit pairs (TDP/TDN) and the $121\ \Omega \pm 1\%$ receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component 82562EZ/ET/EX/EM) as possible. This is because these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 10-39. Intel® 82562EZ/ET/EX/EM Termination



NOTE: Place termination resistors as close to the Intel® 82562ET as possible.

10.3.13.1.3 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the magnetics module, and distance 'B' from the 82562EZ/ET/EX/EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). See [Figure 10-40](#).

Figure 10-40. Critical Dimensions for Component Placement

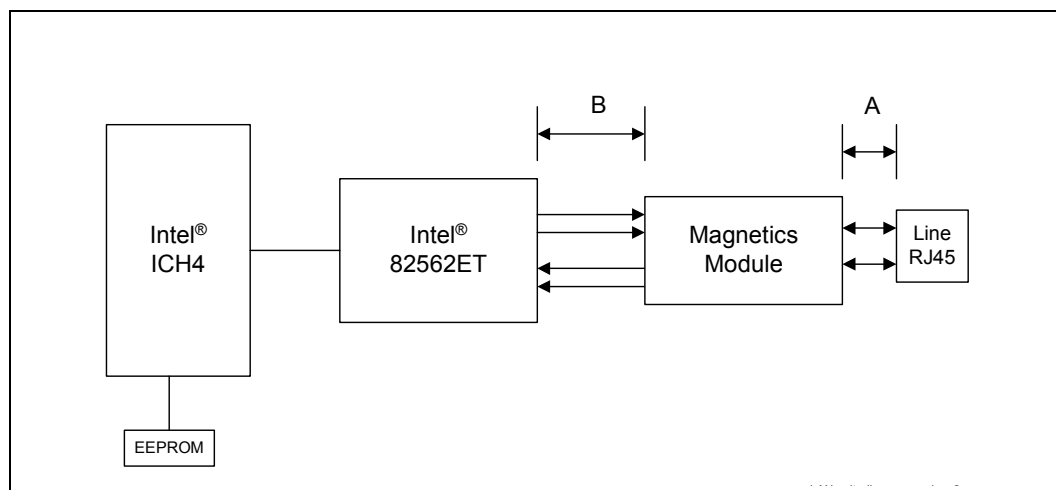


Table 10-24. Dimensions for Figure 10-40

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

Distance from Magnetics Module to RJ45 (Distance A)

The distance A in [Figure 10-40](#) above should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- **Differential Impedance:** The differential impedance should be 100 Ω . The single ended trace impedance will be approximately 60 Ω . However, the differential impedance can also be affected by the spacing between the traces.
- **Trace Symmetry:** Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω –110 Ω should compensate for second order effects.

Distance from Intel® 82562EZ/ET/EX/EM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and of equal length within each differential pair.

10.3.13.1.4 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high-frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and will reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

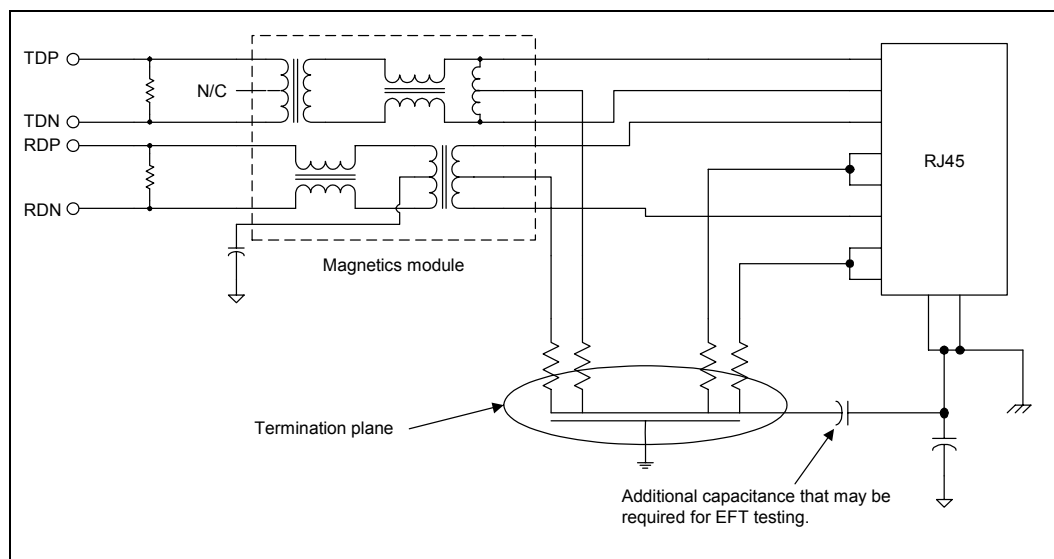
Terminating unused connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.3.13.1.5 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac to meet the EFT requirements.

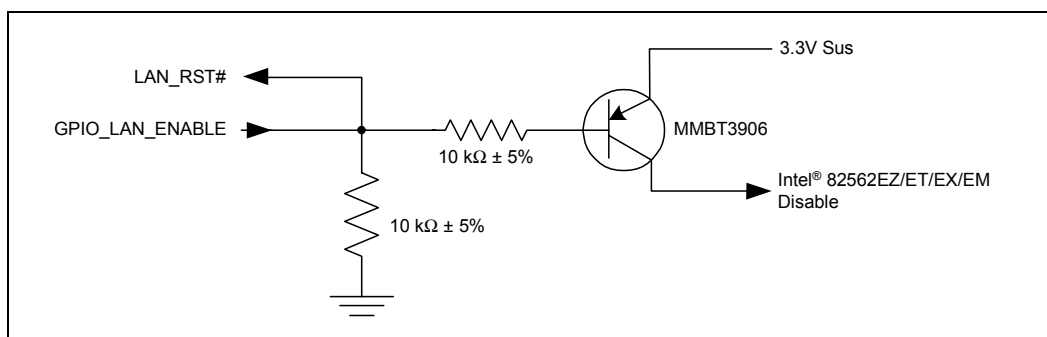
Figure 10-41. Termination Plane



10.3.13.2 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) before assertion of reset (RSM_PWROK). Using a GPIO such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown in Figure 10-42 allows this behavior. The BIOS controlling the GPIO can disable the LAN PHY.

Figure 10-42. Intel® 82562EZ/ET/EX/EM Disable Circuitry



There are 4 pins that are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 10-25 describes the operational/disable features for this design.

The four control signals shown in Table 10-25 should be configured as follows:

- Test_En should be pulled-down through a 100 Ω resistor.
- The remaining 3 control signals should each be connected through 100 Ω series resistors to the common node *Intel® 82562EZ/ET/EX/EM_Disable* of the disable circuit.

Table 10-25. Intel® 82562EZ/ET/EX/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

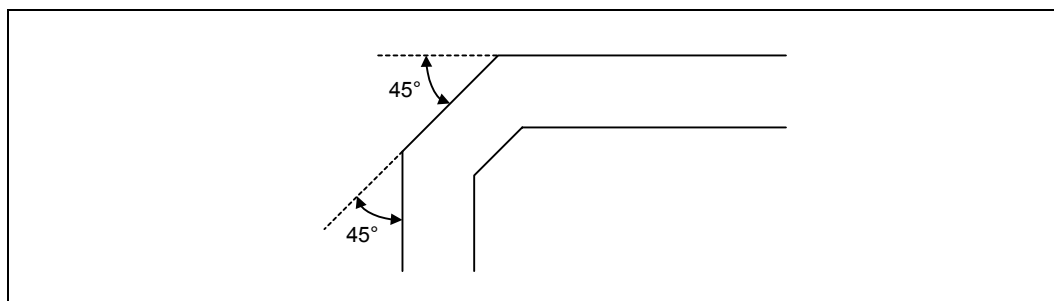
10.3.13.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.3 mil stack-up.):

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two, 45 degree bends. Refer to [Figure 10-43](#).
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 10-43. Trace Routing



10.3.13.3.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be $\sim 100\ \Omega$. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to $10\ \Omega$, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

10.3.13.3.2 Signal Isolation

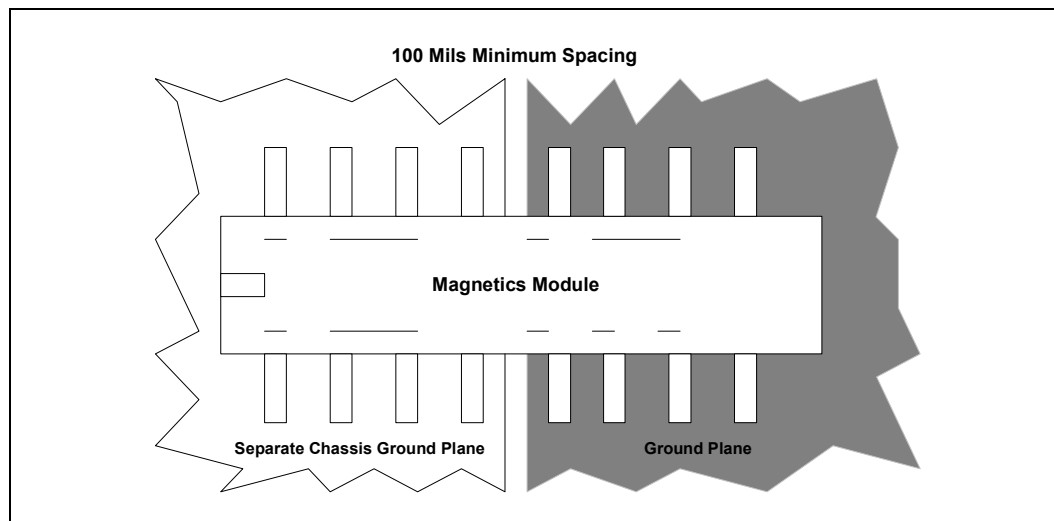
The following are rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from High-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

10.3.13.3.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 10-44. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections, and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.3.13.3.4 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters must be encountered by the other trace at the same distance from the PLC.) Asymmetry can create common-mode noise and can distort the waveforms.
3. Excessive distance between the PLC and the magnetics, or between the magnetics and the RJ45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (= one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω , even when the designers think they've designed for 100 Ω . (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close² to each other, the edge coupling can lower the effective differential impedance by 5 Ω - 20 Ω . A 10 Ω - 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary unless there is some overshoot in 100 Mbps mode.

Note:

1. It is important to keep the two traces within a differential pair close² to each other. Keeping them close² helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.
2. *Close* should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.4 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

10.4.1 FWH Vendors

The following vendors manufacture firmware hubs that conform to the Intel FWH Specification. Contact the vendor directly for information on packaging and density.

- SST <http://www.ssti.com/>
- STM <http://us.st.com/stonline/index.shtml>
- ATMEL <http://www.atmel.com>

10.4.2 FWH Decoupling

A 0.1 μ F capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 μ F capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

10.4.3 In Circuit FWH Programming

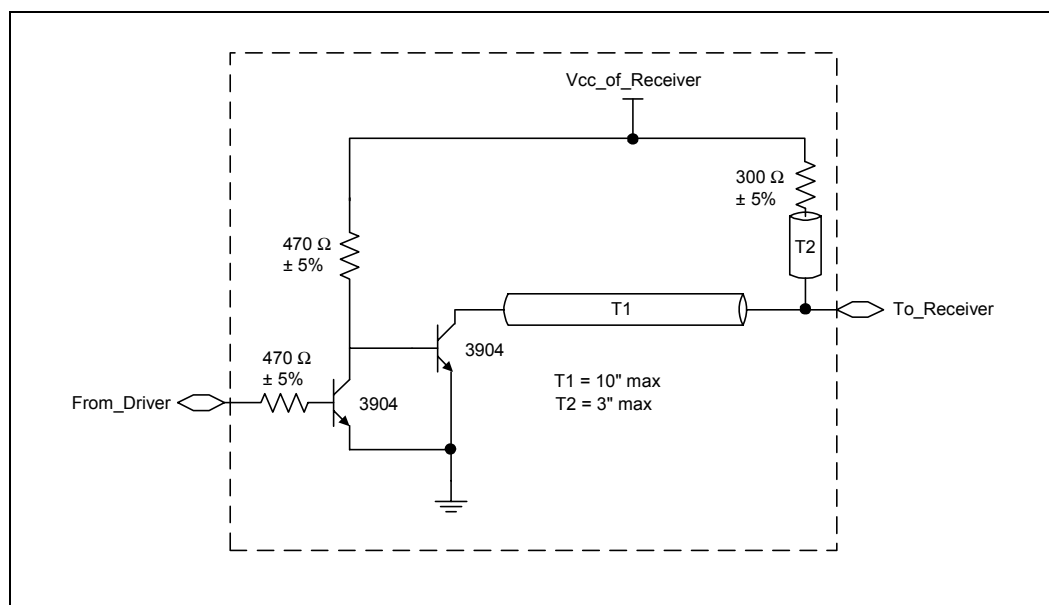
All cycles destined for the FWH will appear on PCI. The ICH4 hub interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.4.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points must be considered because they are **not** consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal must be at a value slightly higher than the VIH min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula $V_{CPU_IOmin} - \text{noise margin}$. Therefore if the V_{CPU_IOmin} of the processor is 1.6 V, the noise margin is 200 mV, and the VIH min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because $1.6 \text{ V} - 0.2 \text{ V} = 1.40 \text{ V}$, which is greater than the 1.35 V minimum of the FWH. If the VIH min of the FWH is 1.45 V there would be an incompatibility, and logic translation would have to be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the VIH min specification is met with ample noise margin.

See [Section 5.4.1.3](#) for INIT# topology and guidelines. The voltage translator circuitry is shown in [Figure 10-45](#).

Figure 10-45. FWH Level Translation Circuit

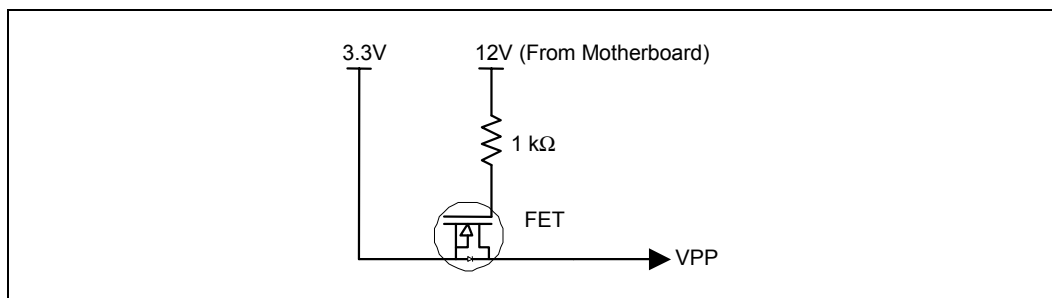


10.4.5 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH supports 12 V V_{PP} for only 80 hours (3.3 V on V_{PP} does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin **must** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit allows testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 10-46. FWH V_{PP} Isolation Circuitry



10.5 Power Management Interface

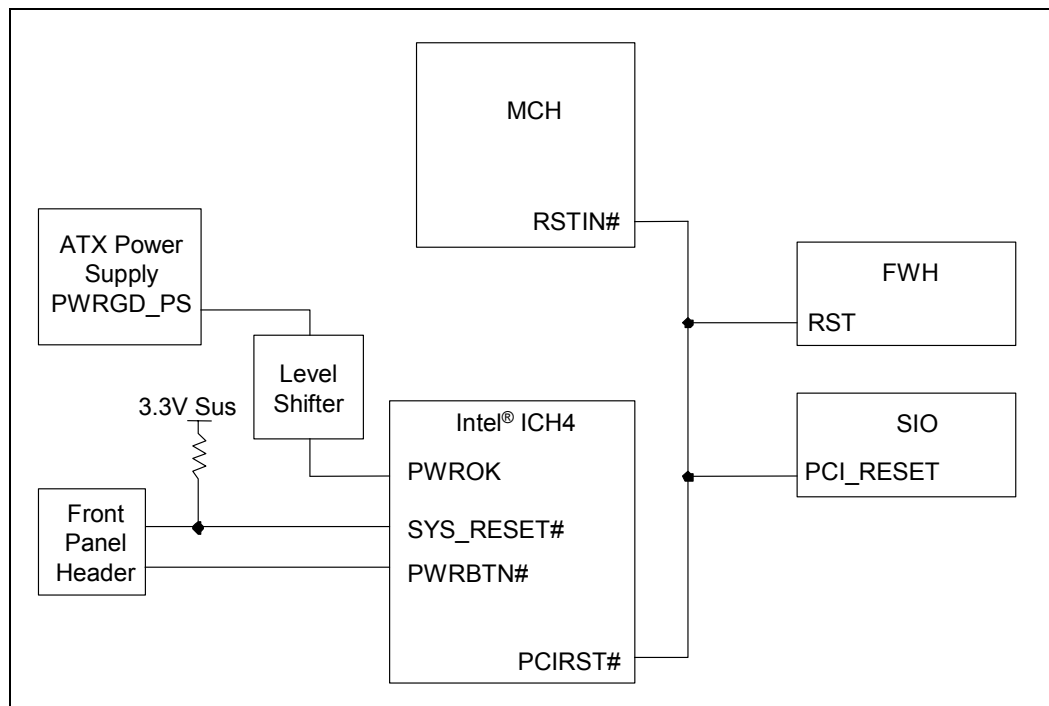
10.5.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 will debounce signals on this pin (16 ms) and will allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from “hanging” by resetting in the middle of a cycle.

10.5.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 k Ω nominal). The ICH4 has 16 ms of internal debounce logic on this pin.

Figure 10-47. SYS_RESET# and PWRBTN# Connection

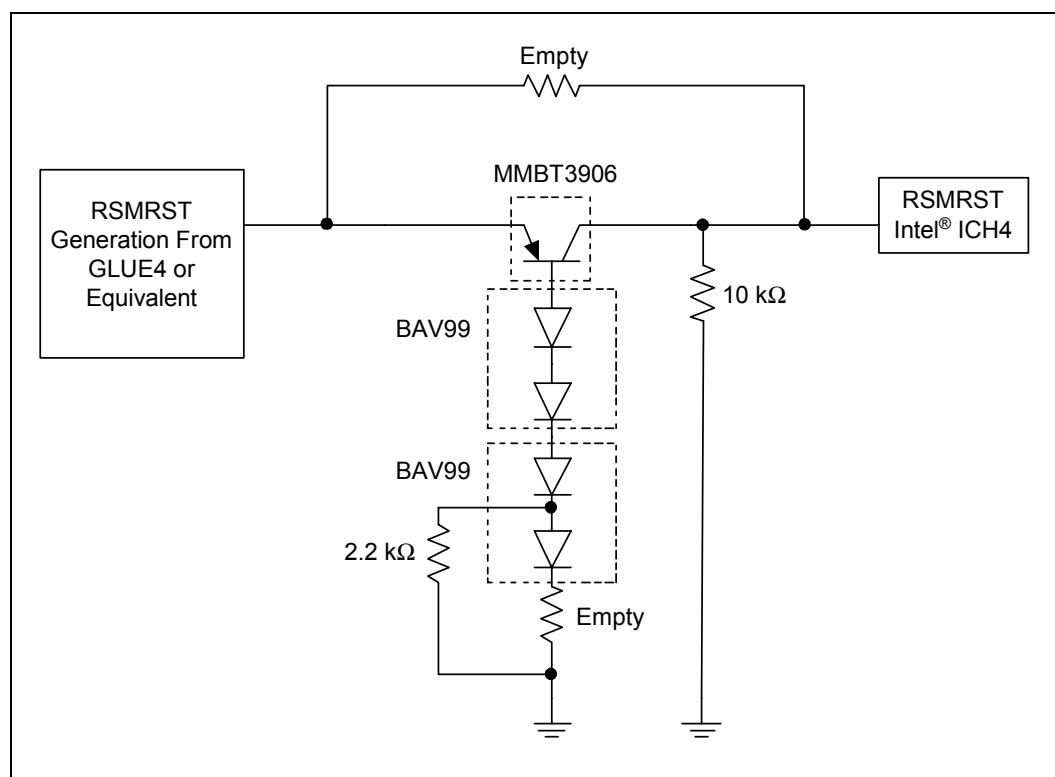


10.6 Power-Well Isolation Control Requirements

The RSMRST# signal of the ICH4 must transition from 20% signal level to 80% signal level and vice-versa in 50 μ s. Slower transitions may result in excessive droop on the VccRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC power cycles, or erroneous intruder bit assertion.

The circuit shown in Figure 10-48 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the 50 μ s rise/fall time.

Figure 10-48. RTC Power Well Isolation Control



10.7 General Purpose I/O

10.7.1 GPIO Summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs. Some of these general purpose inputs and outputs have native functions assigned to them.

Table 10-26. GPIO Summary (Sheet 1 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
0	Yes ²	Core	Input	5 V
1	Yes ²	Core	Input	5 V
2	Yes ²	Core	Input	5 V
3	Yes ²	Core	Input	5 V
4	Yes ²	Core	Input	5 V
5	Yes ²	Core	Input	5 V
6	Yes	Core	Input	5 V
7	Yes	Core	Input	5 V
8	Yes	Resume	Input	3.3 V
9	Yes	Resume	Input	3.3 V
10	Yes	Resume	Input	3.3 V
11	Yes ²	Resume	Input	3.3 V
12	Yes	Resume	Input	3.3 V
13	Yes	Resume	Input	3.3 V
14	Yes	Resume	Output	3.3 V
15	Yes	Resume	Output	3.3 V
16	Yes ²	Core	Output	3.3 V
17	Yes ²	Core	Output	3.3 V
18	Yes	Core	Output	3.3 V
19	Yes	Core	Output	3.3 V
20	Yes	Core	Output	3.3 V
21	Yes	Core	Output	3.3 V
22	Yes	Core	Output open drain	3.3 V
23	Yes	Core	Output	3.3 V
24	Yes	Resume	Input-Output ¹	3.3 V
25	Yes	Resume	Input-Output ¹	3.3 V
26	Yes	Resume	Input-Output ¹	3.3 V
27	Yes	Resume	Input-Output ¹	3.3 V
28	Yes	Resume	Input-Output ¹	3.3 V
29	Yes	Resume	Input-Output ¹	3.3 V
30	Yes	Resume	Input-Output ¹	3.3 V
31	Yes	Resume	Input-Output ¹	3.3 V
32	Yes	Core	Input-Output ¹	3.3 V

Table 10-26. GPIO Summary (Sheet 2 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
33	Yes	Core	Input-Output ¹	3.3 V
34	Yes	Core	Input-Output ¹	3.3 V
35	Yes	Core	Input-Output ¹	3.3 V
36	Yes	Core	Input-Output ¹	3.3 V
37	Yes	Core	Input-Output ¹	3.3 V
38	Yes	Core	Input-Output ¹	3.3 V
39	Yes	Core	Input-Output ¹	3.3 V
40	Yes	Core	Input-Output ¹	3.3 V
41	Yes	Core	Input-Output ¹	3.3 V
42	Yes	Core	Input-Output ¹	3.3 V
43	Yes	Core	Input-Output ¹	3.3 V

NOTES:

1. Defaults as an Output to the ICH4.
2. Can be used as GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

10.8 System Design Considerations

10.8.1 Power Delivery

Table 10-27. Power Delivery Terminology

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
Full-power Operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (CPU stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3), and Soft-off (S5).
Power Rails	An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, and 5 VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® ICH4 Chipset Reference Board.
Core power rail	A power rail that is on only during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ± 5 V, ± 12 V, and + 3.3 V.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is 5 VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived Power Rail	A derived power rail is a power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 VSB is usually derived (on the motherboard) from 5 VSB using a voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation, and from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

10.8.1.1 Intel® ICH4 Reference Board Power Delivery

Figure 10-49. Intel® ICH4 Platform Power Delivery Example

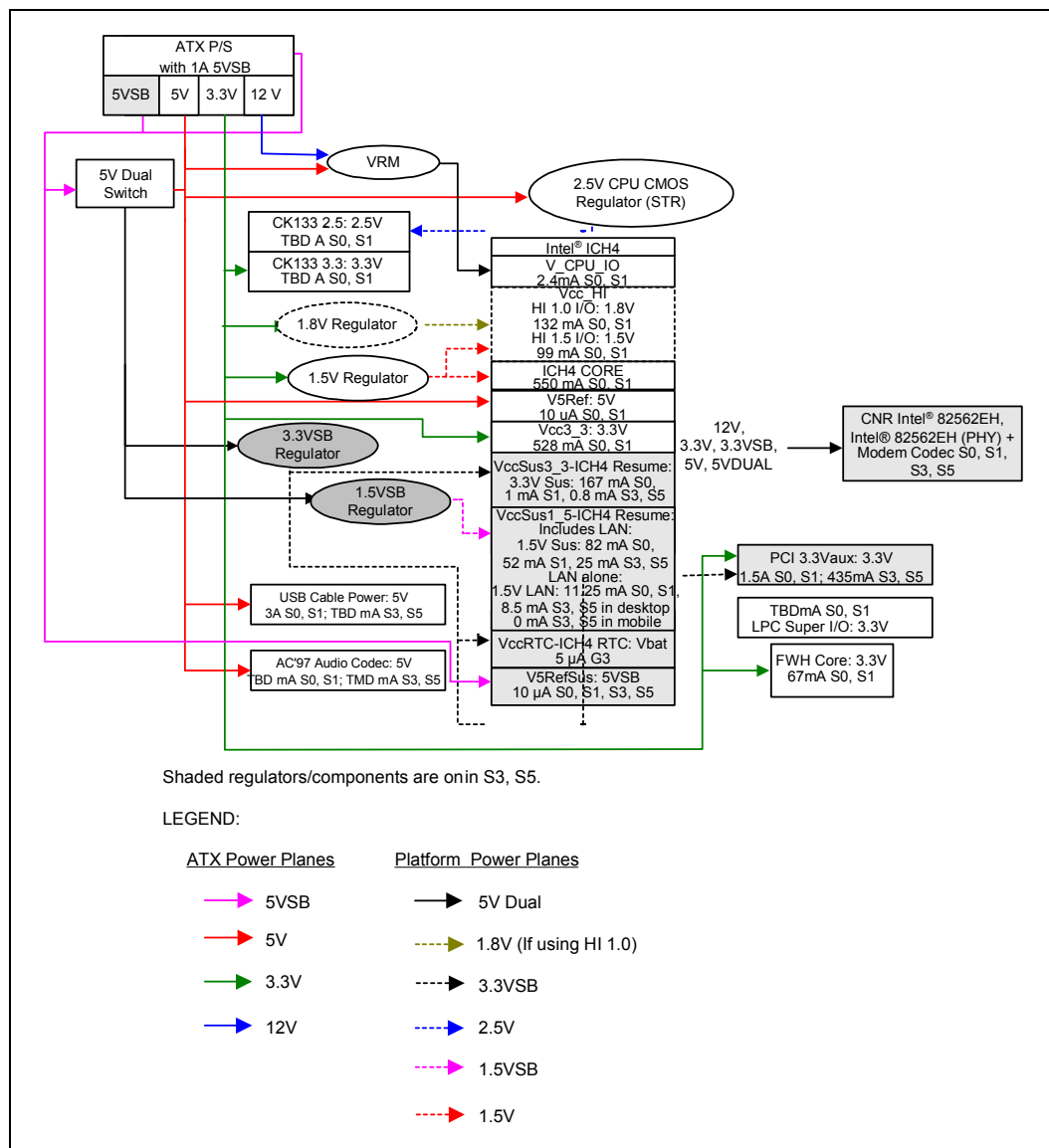


Figure 10-49 shows the suggested power delivery architecture for the ICH4 chipset. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), and USB (USB can be powered only if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device’s power requirements, both in suspend and in full-power. The power requirements must be compared against the power budget supplied by the power supply. Because of the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a dual power rail.

The models given in this Design Guide are only examples. There are many power distribution methods that achieve similar results. It is critical when deviating from these examples in any way to consider the effect of the change.

In addition to the power planes provided by the ATX power supply, an instantly available ICH4 chipset-based system (using Suspend-to-RAM) requires 7 power planes to be generated on the board. The requirements for each power plane are described in this section. In addition to on-board voltage regulators, the ICH4 Chipset Reference Board has a 5 V Dual Switch.

5 V Dual Switch

This switch powers the 5 V Dual plane from the 5 V core ATX supply during full-power operation. During Suspend-to-RAM the 5 V Dual plane is powered from the 5 V Standby power supply. Note that the voltage on the 5 V Dual plane is not 5 V. There is a resistive drop through the 5 V Dual Switch that must be considered. Therefore, **no components** should be connected directly to the 5 V Dual plane. On the ICH4 Reference Board, the only devices connected to the 5 V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an ICH4 chipset-based system that does not support Suspend-to-RAM (STR).

1.8 V

The 1.8 V plane powers the ICH4 Hub Interface 1.0 I/O buffers. If using Hub Interface 1.5, the Hub Interface power signals should be connected to 1.5 V.

Note: This regulator is not required in all designs

1.5 V

The 1.5 V plane powers the ICH4 hub interface 1.5 I/O buffers, as well as other components. For ICH4 power requirements for this rail, see [Table 10-28](#). For decoupling considerations, see [Section 10.8.1.5](#).

Note: This regulator is required in all designs.

3.3 VSB

The 3.3 VSB plane powers the I/O buffers in the resume well of the ICH4 and the PCI 3.3 Vaux suspend power pins. The 3.3 Vaux requirement states that during suspend, the system must deliver 375 mA to each wake-enabled card, and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

Full-power Operation: $375 \text{ mA} * \text{number of PCI slots}$
 Suspend Operation: $375 + 20 * (\text{number of PCI slots} - 1)$

In addition to the PCI 3.3 Vaux, the ICH4 suspend well power requirements must be considered as shown in [Figure 10-49](#).

Note: This regulator is required in all designs.

1.5 VSB

The 1.5 VSB plane powers the logic to the ICH4 resume well.

10.8.1.2 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP_S5# is short (~ 10-100 mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle the short pulse condition. In this case, the power supply will not respond to this event and will never power back up. These power supplies would have to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Because of variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this condition.

10.8.1.3 Intel® ICH4 Analog Power Delivery

There are no analog ICH4 circuits that require filters.

10.8.1.4 Intel® ICH4 Power Delivery

Figure 10-50. Intel® ICH4 Layer 1 Power Delivery

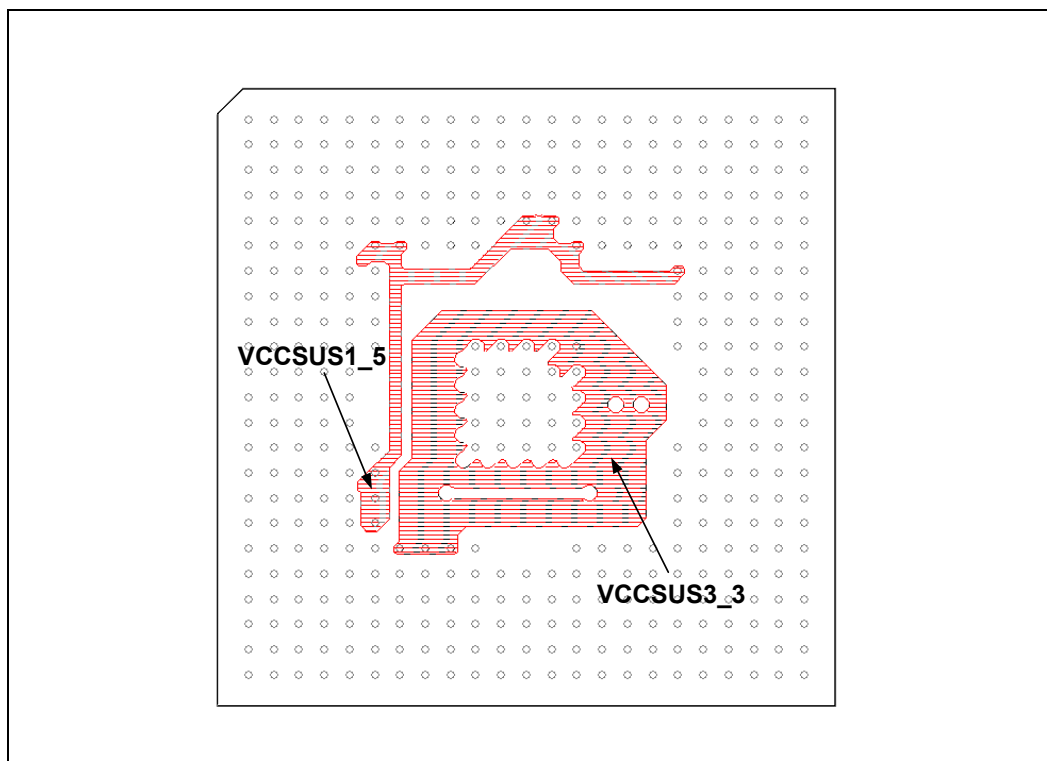


Figure 10-51. Intel® ICH4 Layer 3 Power Delivery

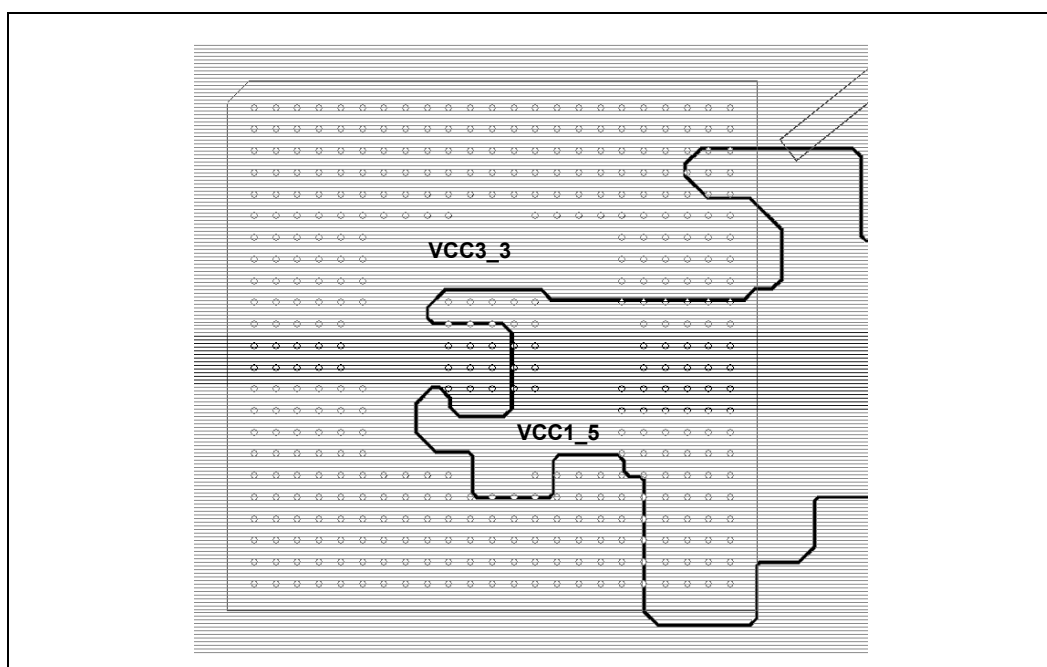


Figure 10-52. Intel® ICH4 Layer 4 Power Delivery

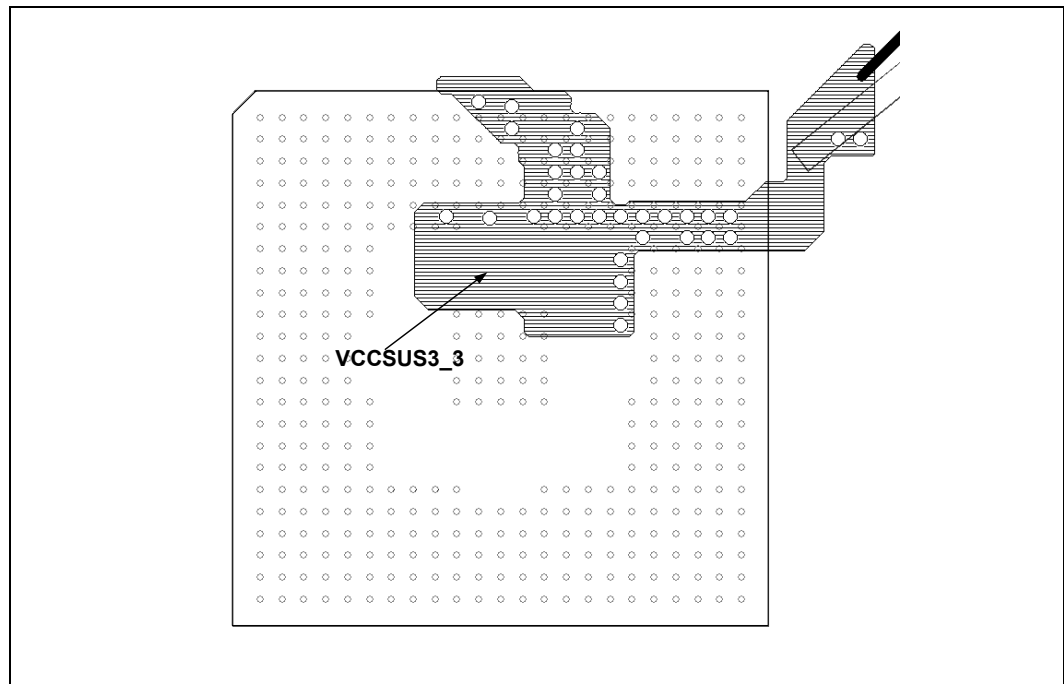
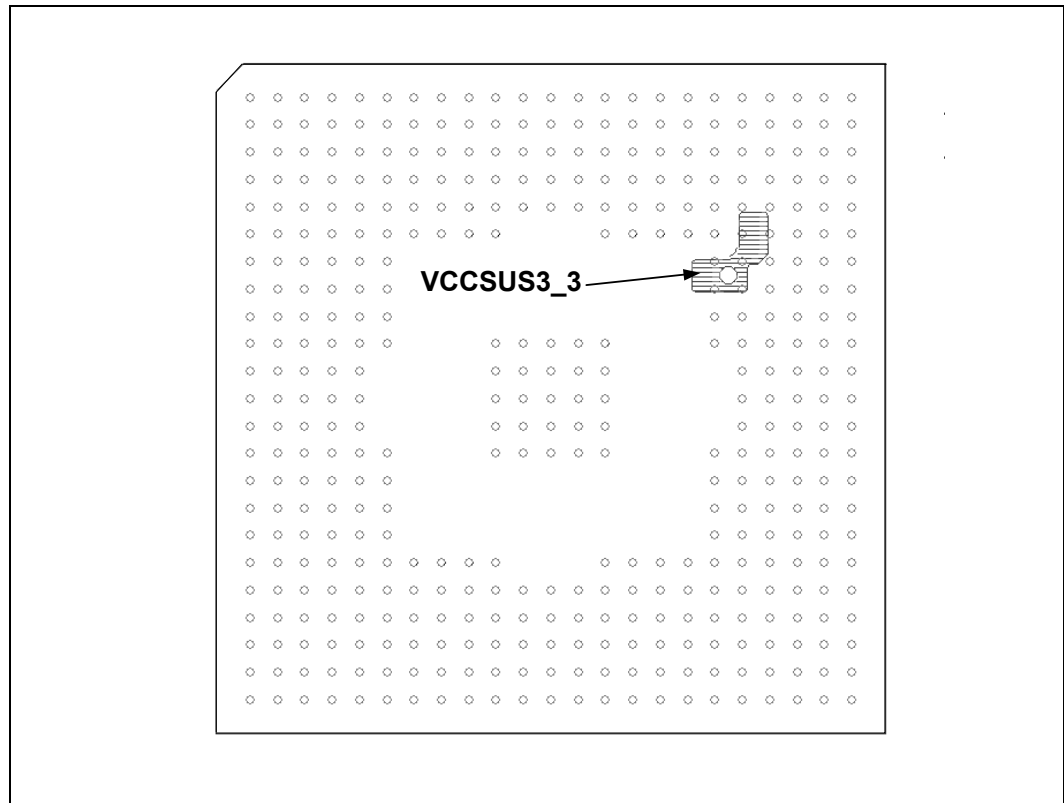


Figure 10-53. Intel® ICH4 Layer 6 Power Delivery



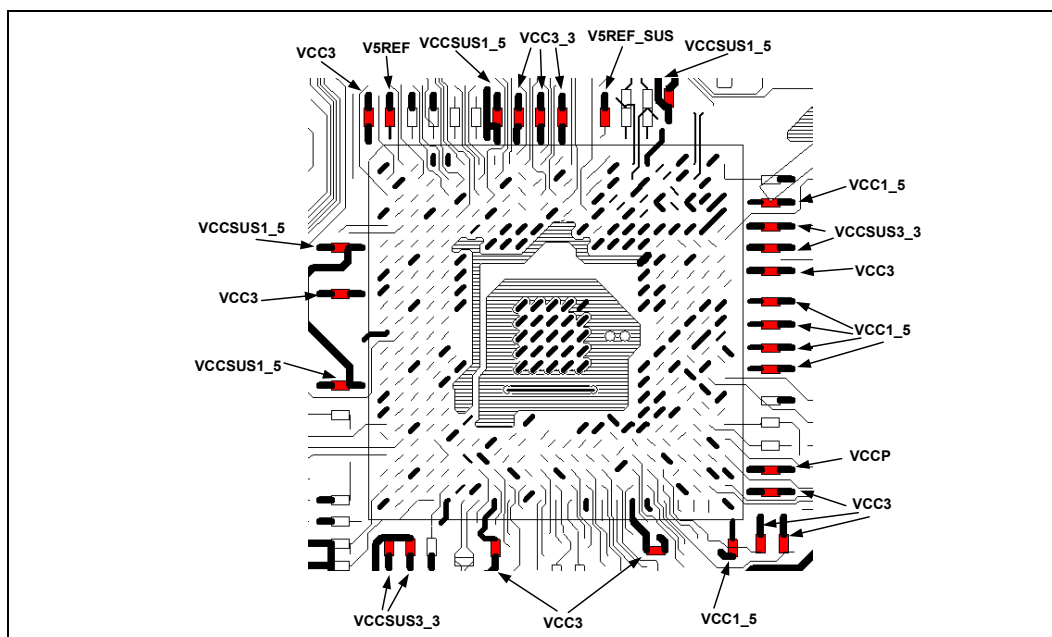
10.8.1.5 Intel® ICH4 Decoupling Recommendations

The ICH4 is capable of generating large current swings when switching between logic high and logic low. This condition can cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in [Table 10-28](#) to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). Rotate caps that are placed over power planes to minimize loop inductance. The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground), and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. It is recommended that for prototype board designs the designer include pads for extra power plane decoupling caps.

Table 10-28. Decoupling Requirements for Intel® ICH4

Pin	Decoupling Requirements	Decoupling Type (Pin type)	Decoupling Placement
VCC3_3	(6) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VccSus3_3	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 μ F	Decoupling Cap (VSS)	Place near ball: AA23
VC1_5	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: K23 and C23
VccSus1_5	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A16 and AC1
V5REF	(1) 0.1 μ F	Decoupling Cap (VSS)	Place near ball: E7
V5REF_Sus	(1) 0.1 μ F	Decoupling Cap (VSS)	Place near ball: A16
VccRTC	(1) 0.1 μ F	Decoupling Cap (VSS)	Place near ball: AB5
VCCHI	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 μ F and (1) 0.01 μ F	Decoupling Cap (VSS)	Place near ball: C22

Figure 10-54. Intel® ICH4 Decoupling Capacitor Placement



10.8.1.6 3.3 V/1.5 V and 3.3 V/1.8 V Power Sequencing

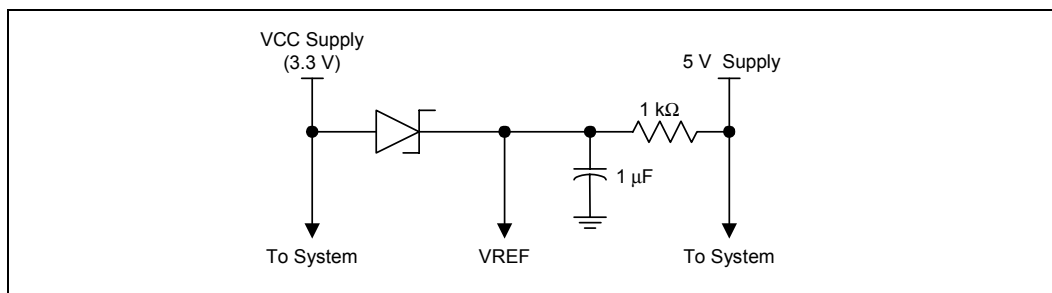
There are no power sequencing requirements for the associated 3.3 V/1.5 V rails or the 3.3 V/1.8 V rail of the ICH4. It is generally good design practice to core power up before or at the same time as the other rails.

10.8.1.7 V5REF/ 3.3 V Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. This rule must be followed to ensure the safety of the ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 10-55 shows a sample implementation of how to satisfy the V5REF/VCC3_3 sequencing rule.

This rule also applies to the stand-by rails, but in most platforms the VccSus3_3 rail is derived from the VccSus5 rail. Therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_SUS will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be observed in the platform design.

Figure 10-55. Example V5REF / 3.3 V Sequencing Circuitry



10.8.1.8 Intel® ICH4 Power Consumption Numbers

Table 10-29 describes ICH4 power consumption.

Table 10-29. Intel® ICH4 Power Consumption Measurements

Power Plane	Maximum Power Consumption				
	S0	S1	S3	S4/S5	G3
1.5 V Core	550 mA	266 mA	N/A	N/A	N/A
3.3 V I/O	528 mA	0.76 mA	N/A	N/A	N/A
1.5 V SUS	82 mA	52 mA	25 mA	25 mA	N/A
3.3 V SUS ¹	167 mA	1 mA	0.8 mA		N/A
VccRTC	N/A	N/A	N/A	N/A	5 µA
V_CPU_IO ²	2.4 mA	2.4 mA	N/A	N/A	N/A
VCCHI ³					
HI 1.0 (1.8 V)	132 mA	132 mA	N/A	N/A	N/A
HI 1.5 (1.5 V)	99 mA	99 mA	N/A	N/A	N/A
V5REF	10 µA	10 µA	N/A	N/A	N/A
V5REF_SUS	10 µA	10 µA	10 µA	10 µA	10 µA

NOTES:

1. 3.3 V SUS S0 assumes maximum USB 2.0 traffic (6 ports populated).
2. V_CPU_IO S1 state primarily due to STPCLK# activity.
3. VCCHI power consumption is dependant on the Hub Interface being used

10.8.2 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The ICH4 thermal design power consumption dissipation is estimated to be 2.9 Watts.

10.8.3 Glue Chip 4 (Intel® ICH4 Glue Chip)

To reduce the component count and BOM cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Voltage translation for DDC to VGA monitor
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

Vendor	Contact Information
Philips Semiconductors	6028 44th Way NE Olympia, WA 98516-2477 Phone: (360) 413-6900 Fax: (360) 438-3606
Fujitsu Microelectronics	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 Phone: 1-800-866-8600 Fax: 1-408-922-9179

NOTE: These vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

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Debug Port

11

Refer to *ITP700 Debug Port Design Guide* for all information necessary to develop a Debug Port on this platform including electrical specifications, mechanical requirements, and all In-Target Probe (ITP) signal layout guidelines.

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Power Distribution Guidelines

12

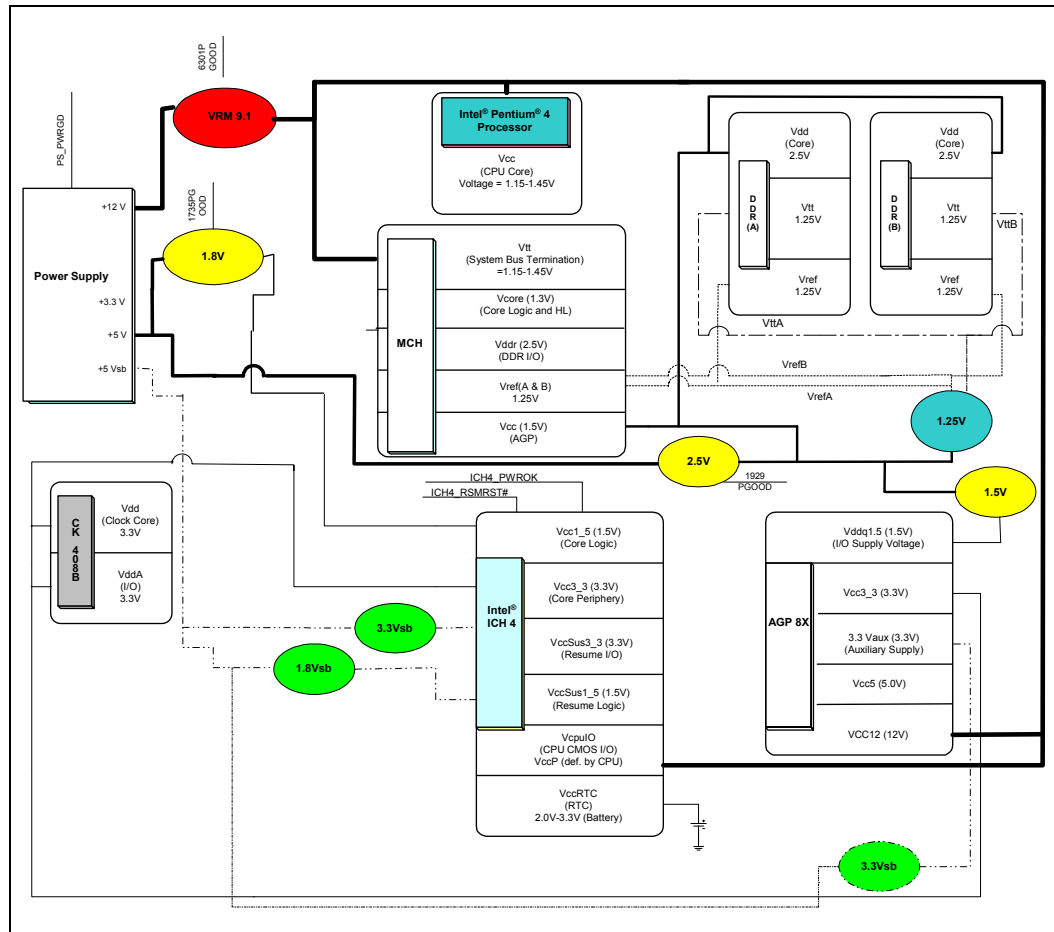
Table 12-1. Power Delivery Terminology

Term	Definition
Full-Power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant) state.
Power Rails	A power supply has five power rails: +12 V, -12 V, +5 V, +3.3 V, +5VSB. In addition to these power rails coming off the power supply, several other power rails are created by voltage regulators on the E7205 chipset Reference Board.
Core Power	A power rail that is only on during full-power operation. These power rails are on when rail the active-low PSON signal is asserted to the power supply. The core power rails that are distributed directly from the power supply are: +12 V, -12 V, +5 V, and +3.3 V.
Standby Power Rail	Standby power is supplied by the power supply during times when the system is powered down. The purpose is to maintain functions that must always be enabled, such as the date and time-of-day within the BIOS. A 5VSB power rail is provided by the power supply.
Derived Power	A derived power rail is any power rail generated from another power rail using a Rail on-board voltage regulator. For example, +2.5 V is derived from a +5 V power rail using a voltage regulator.

12.1 Customer Reference Board Power Delivery

Figure 12-1 shows the power delivery architecture for the Customer Reference Board.

Figure 12-1. Intel® E7205 Chipset Power Delivery Example



NOTE: The examples given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way to consider the effects of the change.

12.1.1 Voltage Rail and Max Current Specifications

12.1.1.1 Processor VID

The processor core voltage power plane is used to power the processors. The core voltage operates between 1.3 V and 1.5 V. The VRM or VRD equivalent will be a VRM 9.1 design. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*. A VRM 9.1 compatible design is required for all E7205 chipset platforms.

12.1.1.2 2.5 V

The 2.5 V power plane is used to power the DDR DRAM core, the MCH DDR I/O ring, and the 2.5 V-to-1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support the specification listed in [Table 12-2](#). This switching regulator receives its input directly from the 5 V power rail of the power supply. Refer to the DRAM specification for vendor specific maximum current.

12.1.1.3 1.5 V

The 1.5 V power plane powers the AGP 8X component and the AGP 8X interface located on the MCH. Refer to [Table 12-2](#) for details.

12.1.1.4 1.25 V

The voltage regulator produces two 1.25 V rails. One is for VREF, and the other is for V_{TERM} . The switching regulator divides the 2.5 V power rail by two to drive 1.25 V reference voltage. This provides some common mode noise rejection between the DDR termination and I/O voltages. Because of power sequencing requirements, the 1.25 V power rail must be derived by the 2.5 V regulator. Refer to [Table 12-2](#) for details.

12.1.1.5 1.8 V

The 1.8 V power plane is created using a switching regulator that sources from the 5 V power rail on the power supply. The 1.8 V plane powers the ICH4 core logic. Refer to [Table 12-2](#) for maximum current specification.

12.1.1.6 1.3 V

The 1.3 V power plane powers the MCH core logic. Refer to [Table 12-2](#) for maximum current specification.

12.1.1.7 5 VSB

The 5 VSB power plane comes directly from the 5 VSB power rail and has two functions: to provide power to resume functions in I/O devices off of the ICH4, and to provide 1.8 VSB power through a linear regulator. Refer to [Table 12-2](#) for maximum current specification.

12.1.1.8 3.3 VSB

The 3.3 VSB power plane is the output of a 5 VSB-to-3.3 VSB voltage regulator. The power plane is used solely for the resume I/O features of the ICH4. Refer to [Table 12-2](#) for maximum current specification.

12.1.1.9 1.8 VSB

As already stated, the 1.8 VSB provides power to the resume logic within the ICH4. Refer to [Table 12-2](#) for maximum current specification.

Table 12-2. Platform Component Max Current Specifications

Platform Component	Voltage Rail (V) / Max Current Specification (A)					
	1.3	1.25	1.4	1.5	2.5	3.3
MCH	3.20		2.10	0.6	6.80	–
Intel® ICH4	–	–	–	0.97	–	0.61
DDR	–	6.20	–	–	21.00	
CK 408	–	–	–	–	–	0.36
Rail Totals (A)	3.20	6.20	2.10	1.03	26.80	0.97

12.2 Power Requirements

Intel recommends using an *Intel® Pentium® 4 Processor VR-Down Design Guidelines*-compliant regulator for the processor system board designs. An *Intel® Pentium® 4 Processor VR-Down Design Guidelines*-compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure voltage fluctuations remain within the specifications in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. See [Table 12-3](#) for recommendations on the amount of decoupling needed.

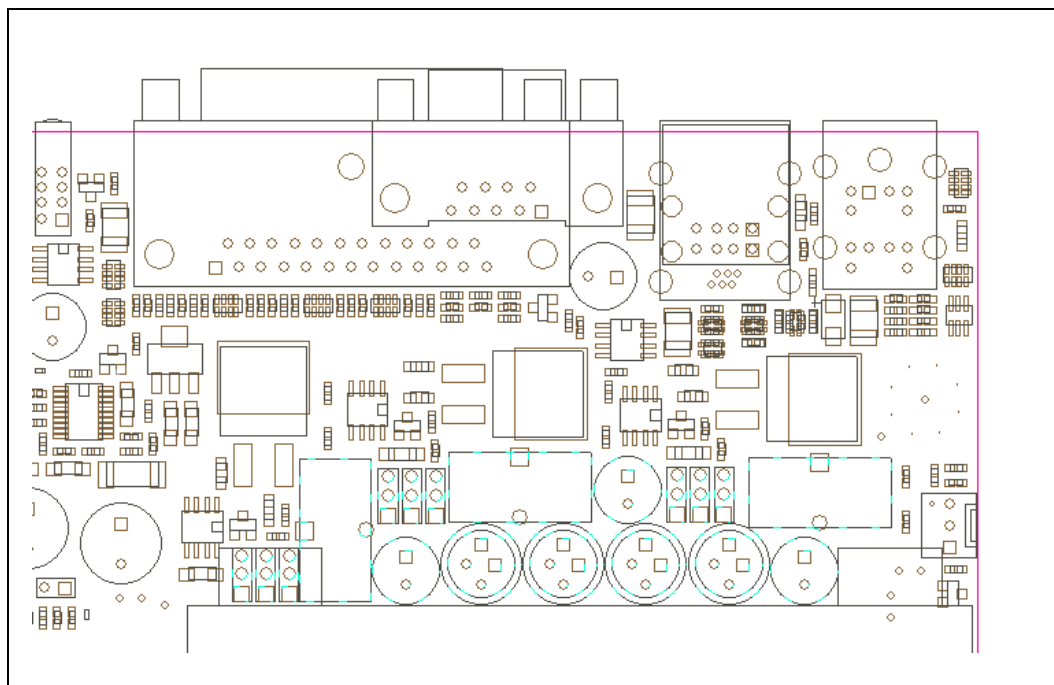
Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*.

The voltage tolerance of the loadlines contained in these documents help the system designer achieve a flexible motherboard design solution for all frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower level using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses ($I \times R$). More important however, an on-board regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. [Figure 12-2](#) shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in [Figure 3-1](#). North refers to the side of the processor closest to the back panel, and South refers to the side of the processor closest to the system memory.

Figure 12-2. VR Component Placement



12.3 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in [Table 12-3](#).

Table 12-3. Decoupling Requirements

Capacitance	ESR (each)	ESL (each)	Ripple Current Rating (each)	Notes
11 OS-CONs*, 560 μ F	9 m Ω , max	4 nH, max	4.080 A _{rms}	1
38 1206 package, 10 μ F	3.97 m Ω , typ	880 pH, typ		1

NOTE:

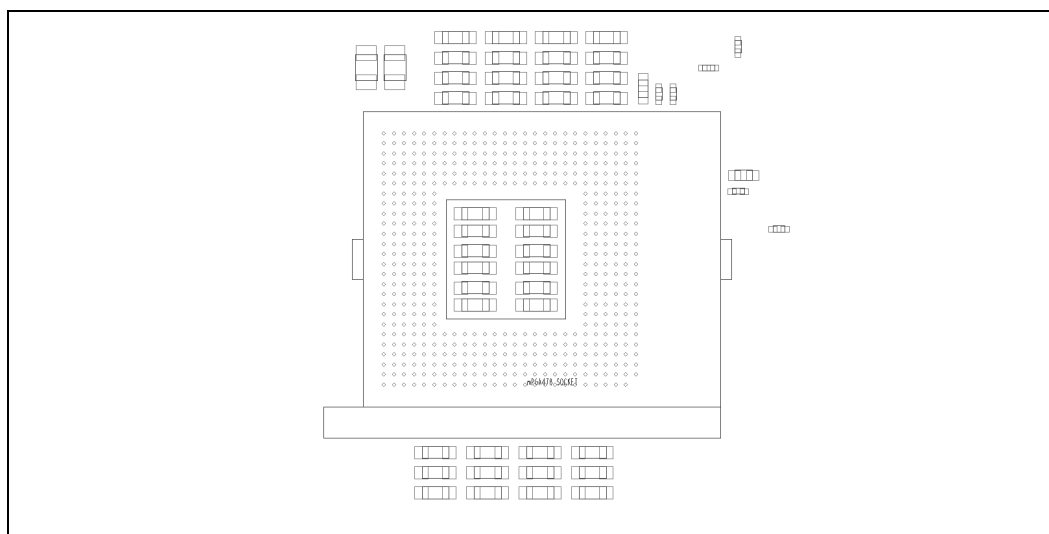
1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.

The decoupling should be placed as close as possible to the processor power pins. [Table 12-4](#) and [Figure 12-3](#) illustrate the recommended placement.

Table 12-4. Decoupling Locations

Type	Number	Location
560 μ F OS-CONs*	6	North side of the processor as close as possible to the keep-out area for the retention mechanism
560 μ F OS-CONs*	5	South side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 μ F	14	North side of the processor as close as possible to the processor socket
1206 package, 10 μ F	10	Inside the processor socket cavity
1206 package, 10 μ F	14	South side of the processor as close as possible to the processor socket

Figure 12-3. Processor Decoupling Placement



12.4 Layout

All six layers in the processor area should be used for power delivery. Four layers should be used for VCC_CPU, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor because of the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompass the power delivery part of the processor pin field are required. [Figure 12-4](#) through [Figure 12-6](#) show examples of how to use shapes to deliver power to the processor.

Figure 12-4. Top Layer Plane

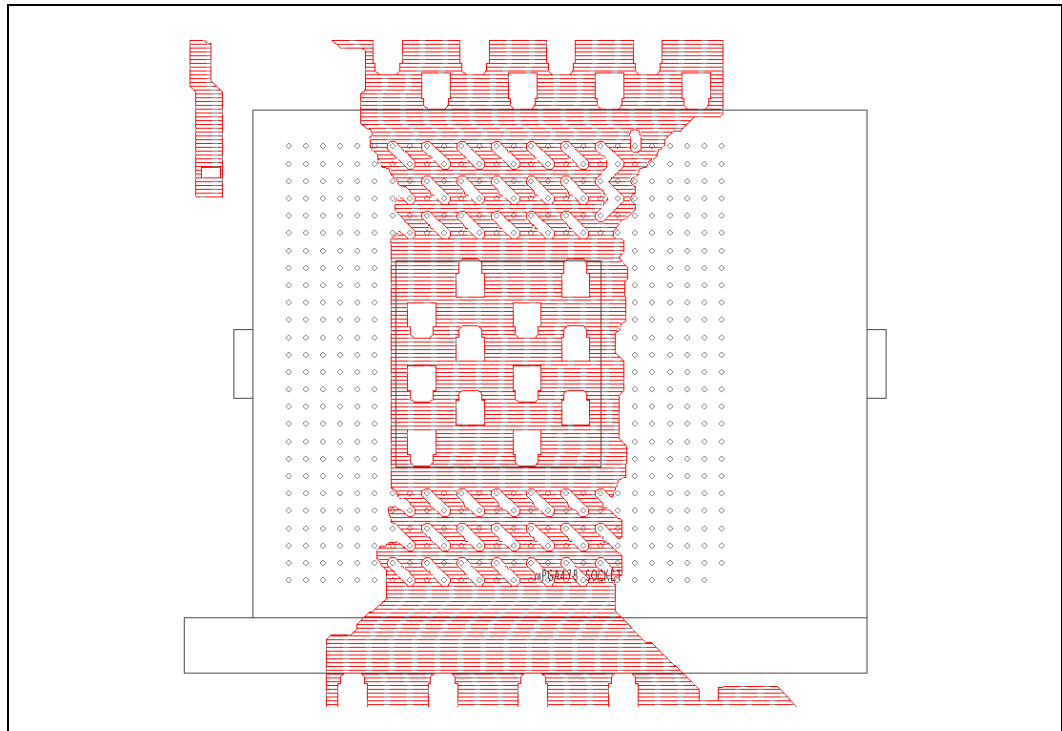


Figure 12-5. Layer 3 Plane

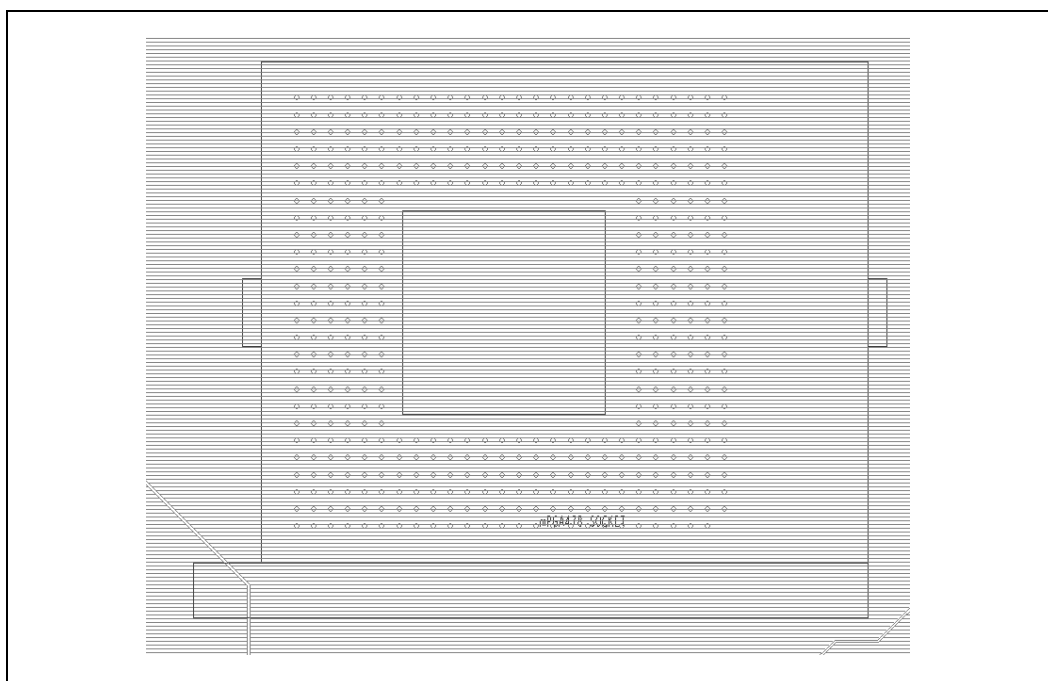
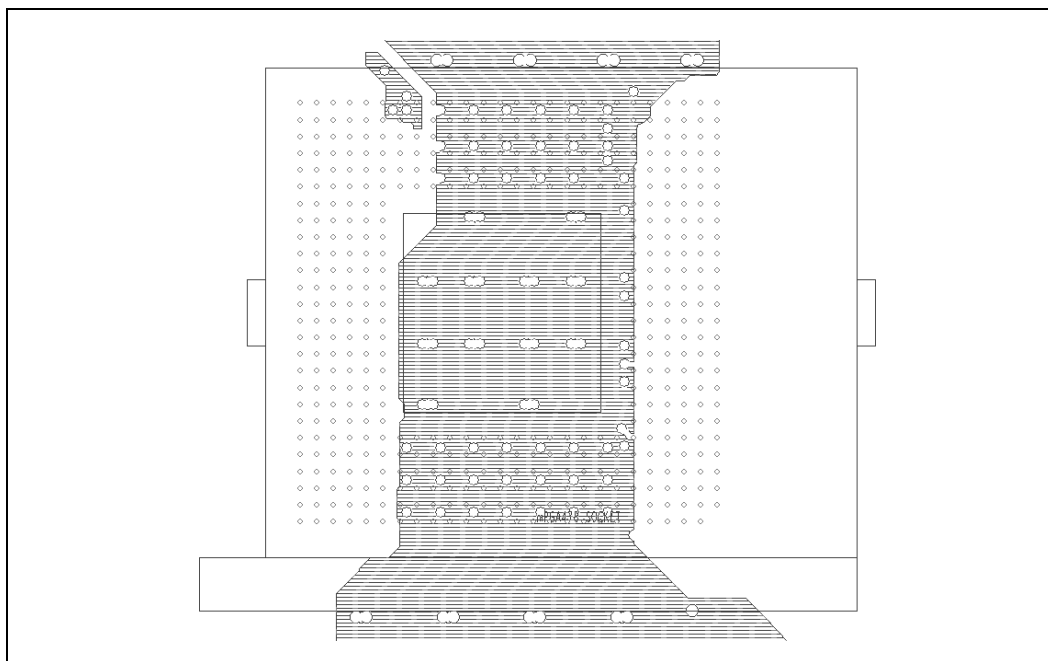
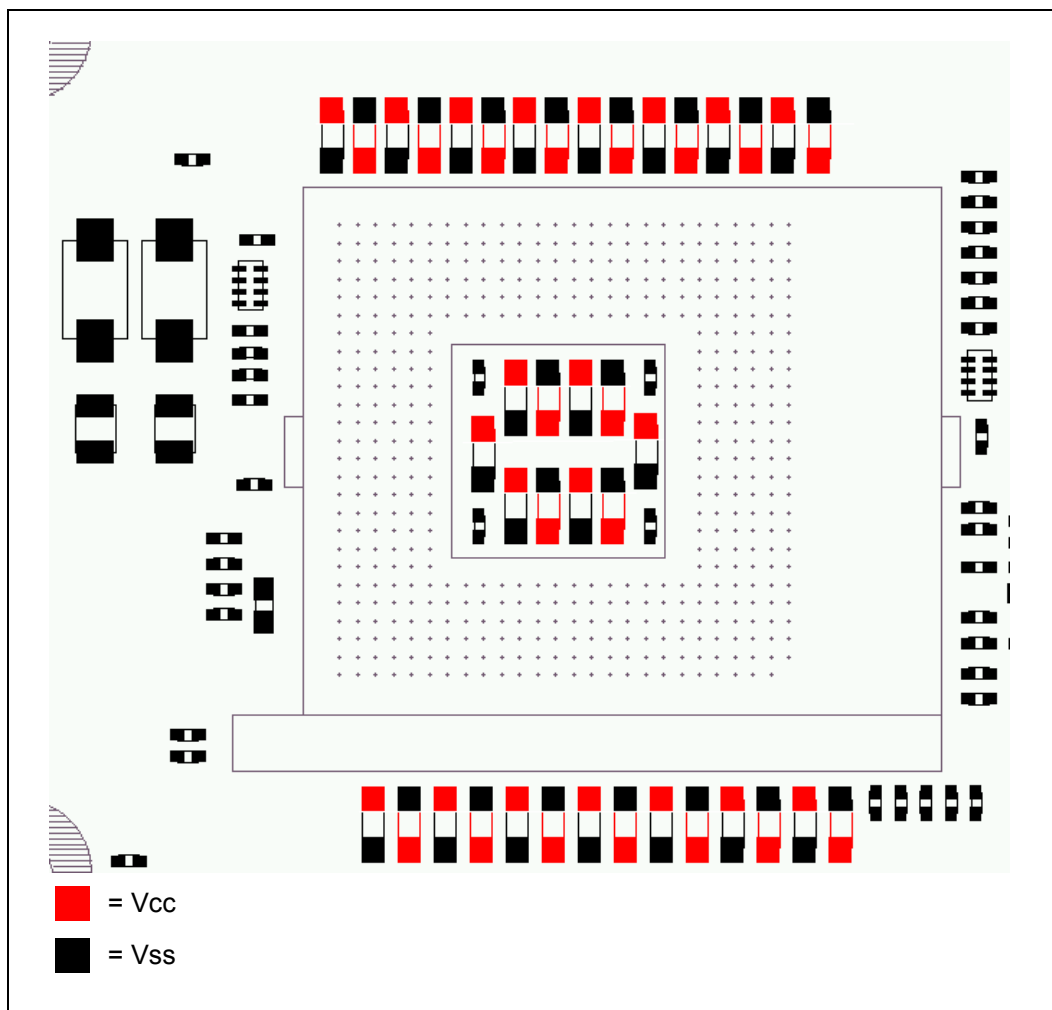


Figure 12-6. Bottom Layer Plane



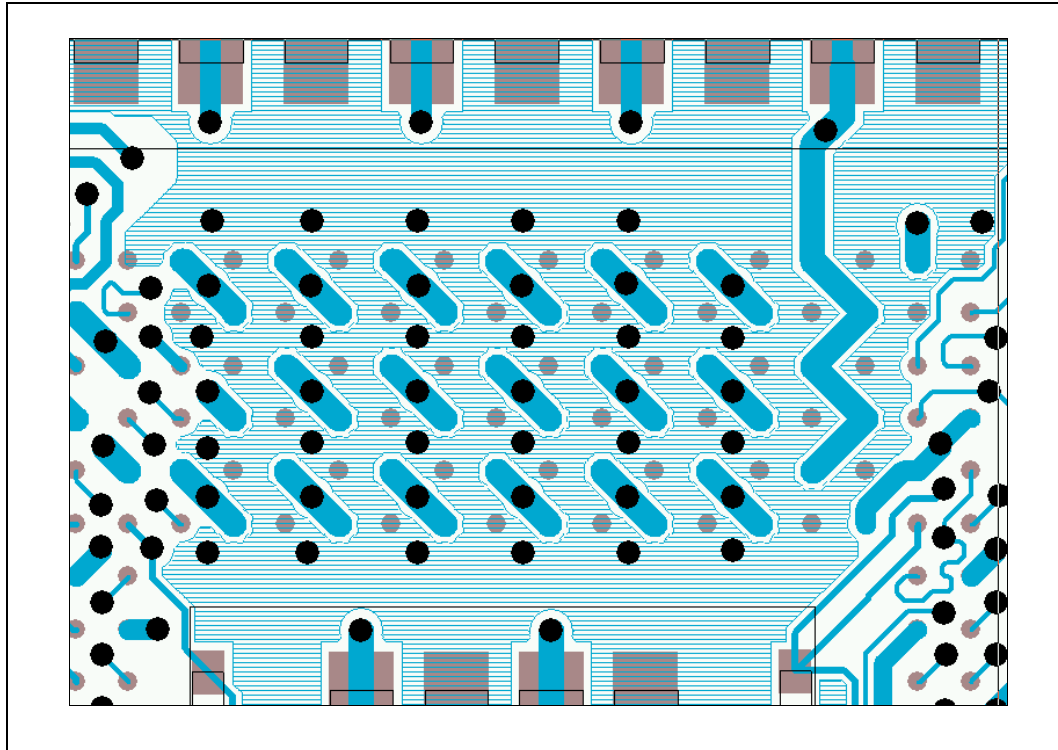
The high-frequency decoupling capacitors should be placed with alternating VCC_CPU and VSS to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 12-7.

Figure 12-7. Alternating VCC_CPU/VSS Capacitor Placement



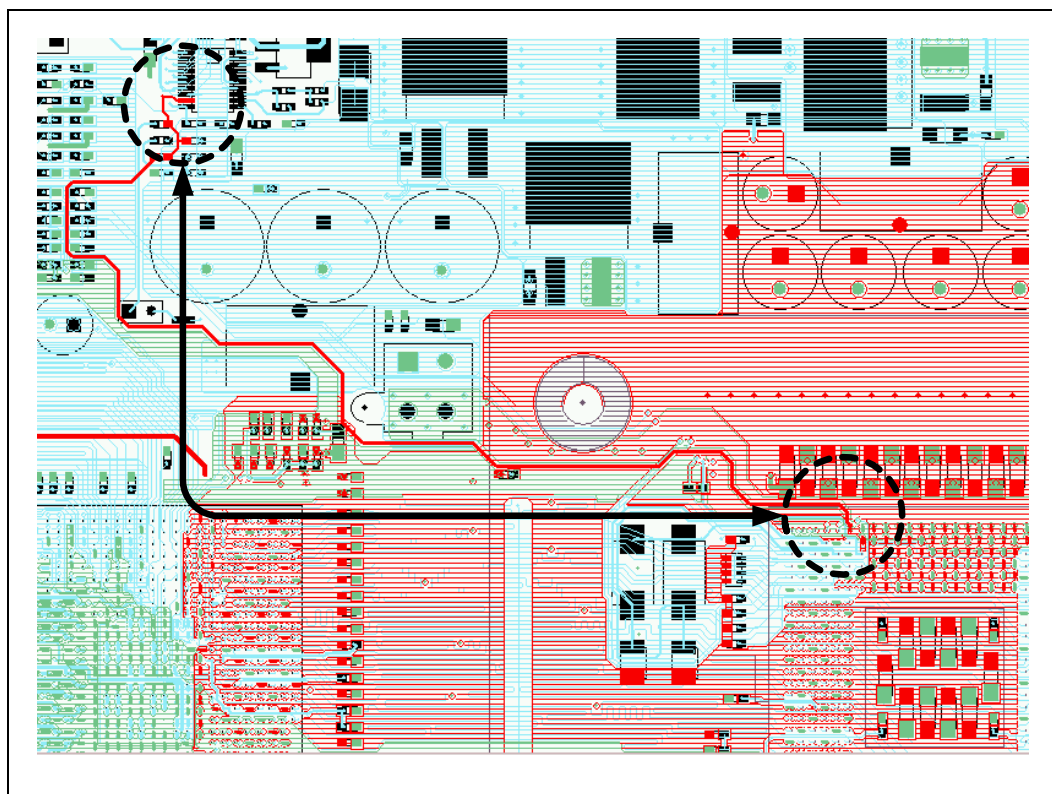
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias be shared for every two processor ground pins and for every two processor power pins. [Figure 12-8](#) illustrates this via sharing.

Figure 12-8. Shared Power and Ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor in the 478 Pin Package VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS), and should be validated from these pins. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. [Figure 12-9](#) shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

Figure 12-9. Routing of VR Feedback Signal



12.5 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution be able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

12.5.1 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins, body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in [Figure 12-10](#).

Figure 12-10. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

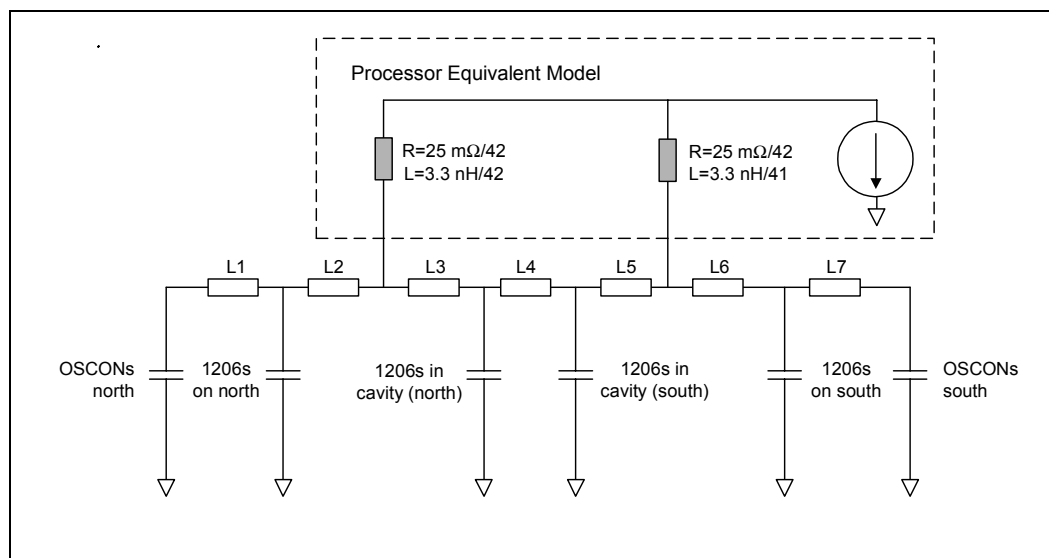


Table 12-5 lists model parameters for the system board shown in Figure 12-10.

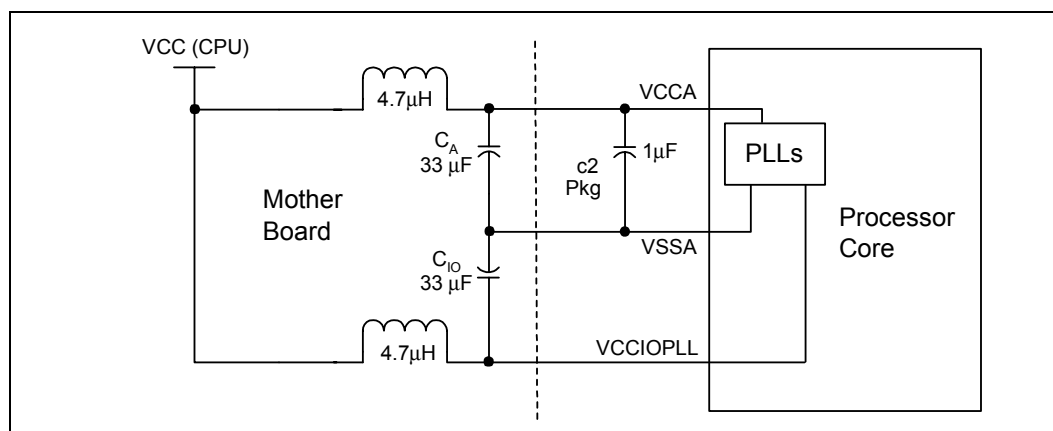
Table 12-5. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance
L1	0.22 mΩ
L2	0.283 mΩ
L3	0.283 mΩ
L4	0.144 mΩ
L5	0.283 mΩ
L6	0.375 mΩ
L7	

12.6 Filter Specifications for VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system—it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from VCC. The general desired filter topology is shown in Figure 12-11. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 12-11. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, this document addresses the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

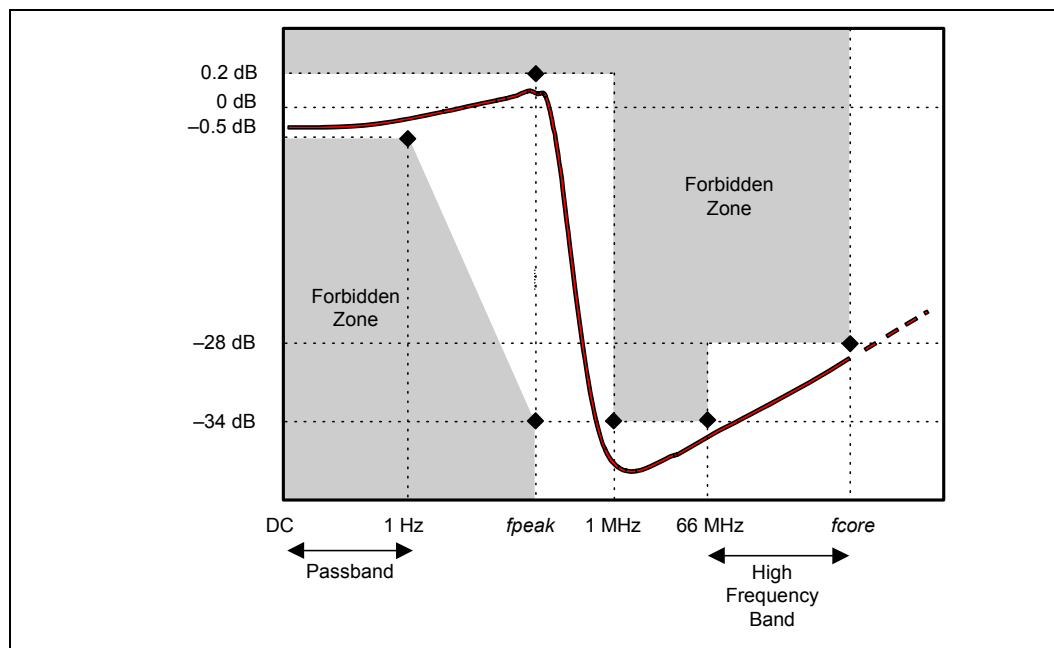
Note: The 1 μF package capacitor shown in Figure 12-11 does not exist on the Pentium 4 processors in the 478-pin package. It is present for the Pentium 4 processors with 512-KB L2 cache on 0.13 micron process only.

The AC low-pass recommendation, with input at VCC and output measured across the capacitor (C_A or C_{IO} in Figure 12-11), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in Figure 12-12.

Figure 12-12. Filter Recommendation



NOTES:

1. Diagram not to scale.
2. No specification for frequencies beyond f_{core} (core frequency).
3. f_{peak} , if existent, should be less than 0.05 MHz.

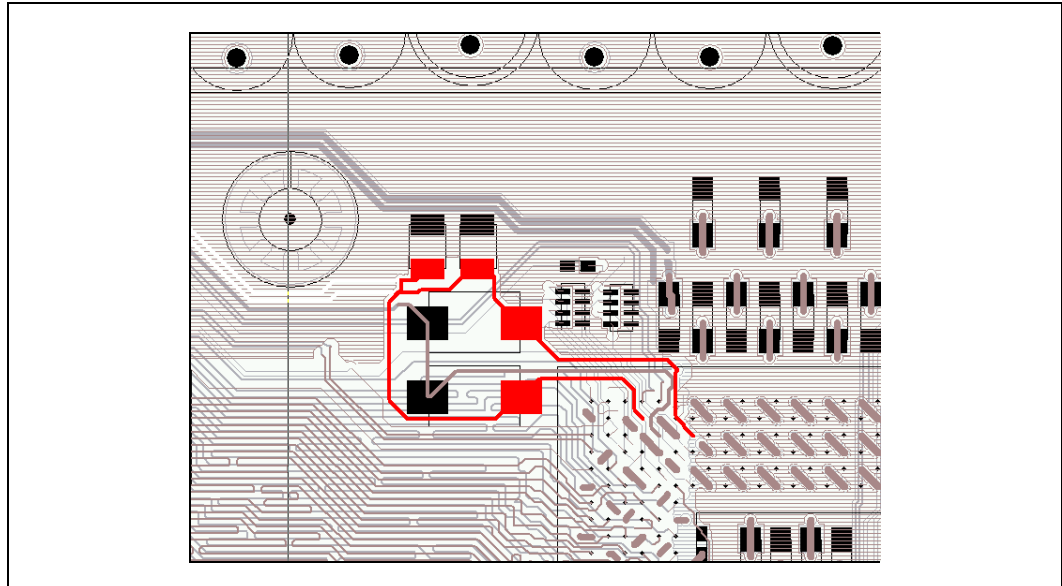
Other recommendations:

- Use shielded type inductors to minimize crosstalk.
- Capacitors for the filter can be any value between 22 μ F and 100 μ F as long as components with $ESL \leq 5$ nH and $ESR < 0.3 \Omega$ are used.
- Values of either 4.7 μ H or 10 μ H may be used for the inductor.
- Filter should support DC current > 60 mA
- DC voltage drop from VCC to VCCA should be < 60 mV.
- To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω

Other routing requirements:

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in [Figure 12-13](#).
- VCCA route should be parallel and next to VSSA route (minimize loop area).
- A minimum of a 12 mil trace should be used to route from the filter to the processor pins.
- L should be close to C.

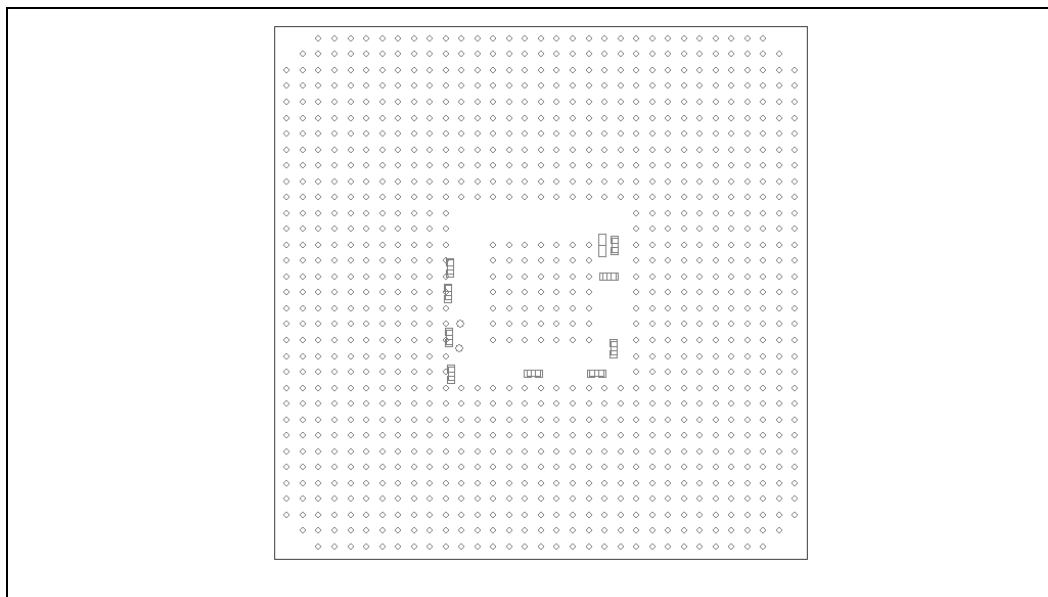
Figure 12-13. Example Component Placement for PLL Filter



12.7 MCH Power Delivery Requirements

The following guidelines are recommended for optimum MCH power delivery. The main focus of these guidelines is to minimize power noise and signal integrity problems to the E7205 chipset. The following guidelines are not intended to replace thorough system validation on E7205 chipset-based products.

Figure 12-14. MCH Decoupling Placement (Backside View)



12.7.1 2.5 V Power Plane (DDR)

See [Section 6.3.1.1](#).

12.7.2 1.25 V Power Plane (DDR_VTT)

See [Section 6.4.3](#) and [Section 6.4.2](#).

12.7.3 VCC_CPU

A maximum of five, 0.1 μ F capacitors are recommended (at least four (4) with 900 pH to 1.1 nH inductance must be placed under the MCH) for FSB 1.45 V power plane decoupling. The designer should evenly distribute placement of decoupling capacitors among the FSB interface signal field. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of nine evenly-spaced capacitors for FSB (at least seven must be within 0.5 inch of the outer row of balls to the MCH).

12.7.4 1.5 V Power Plane (AGP)

Ten 0.1 μ F high-frequency decoupling capacitors (package 0603) should be placed near the MCH to assist in the signal integrity areas of via stitching and return paths for the read condition of the AGP interface.

12.7.5 1.3 V Power Plane (VCC_CORE)

There are no additional decoupling requirements for the 1.3 V power plane.

12.7.6 Filter Specifications

VCCAHI and VCCAFSB are required by the MCH's internal PLLs and DLLs. VCCAHI is created by using a low pass filter on VCC1_3. VCCAFSB is created by using a low pass filter on VCC1_3. The MCH has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter is detrimental to a system—it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The filter topologies are shown in Figure 12-15 through Figure 12-16.

When designing the VCCAHI and VCCAFSB filters (Figure 12-15 and Figure 12-16) make sure that the following guidelines are followed:

- One Inductor 100 nH close to the edge of the package (within 1 inch from the die).
- One LF capacitor 100 μ F or 150 μ F close to the edge of the package.
- At least one Low ESL HF capacitor, 0.1 μ F on the backside of the motherboard under the die.

Figure 12-15. MCH Filter Topology for VCCAHI (HUB Interface)

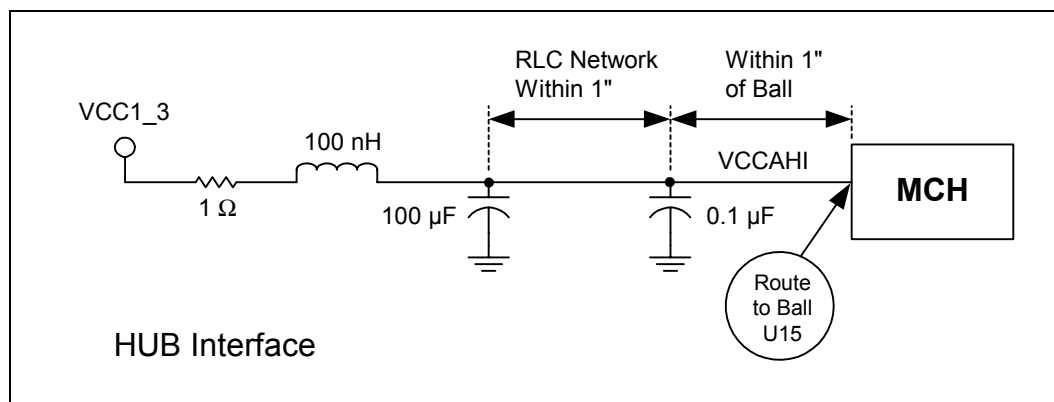
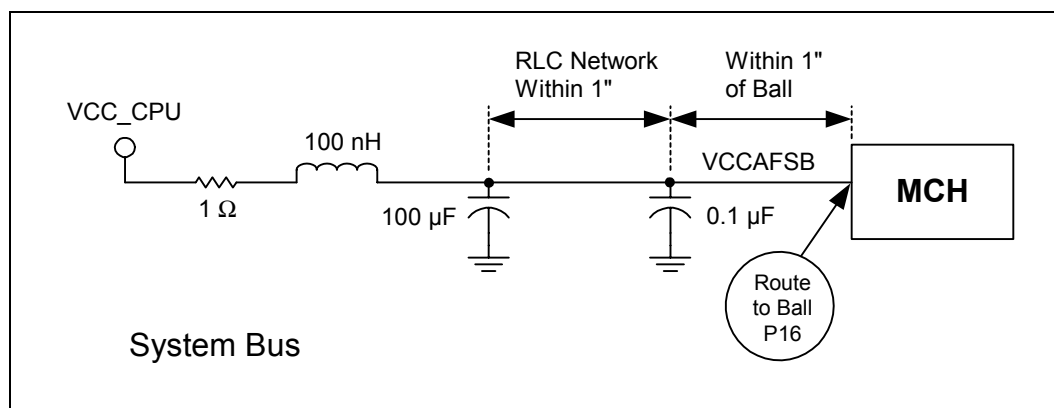


Figure 12-16. MCH Filter Topology for VCCAFSB (System Bus)



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Mechanical Design Considerations 13

13.1 Retention Mechanism Placement and Keep-Outs

The RM requires a keep-out zone for a limited component height area under the RM as shown in Figure 13-1 and Figure 13-2. The figures show the relationship between the RM mounting holes and pin one of the socket, and show the keep-out requirements.

The retention holes should be non-plated holes. The retention holes should have a primary and secondary side route keep-out area of 0.409 inches diameter.

For heatsink volumetric information, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

Figure 13-1. Retention Mechanism Keep-Out

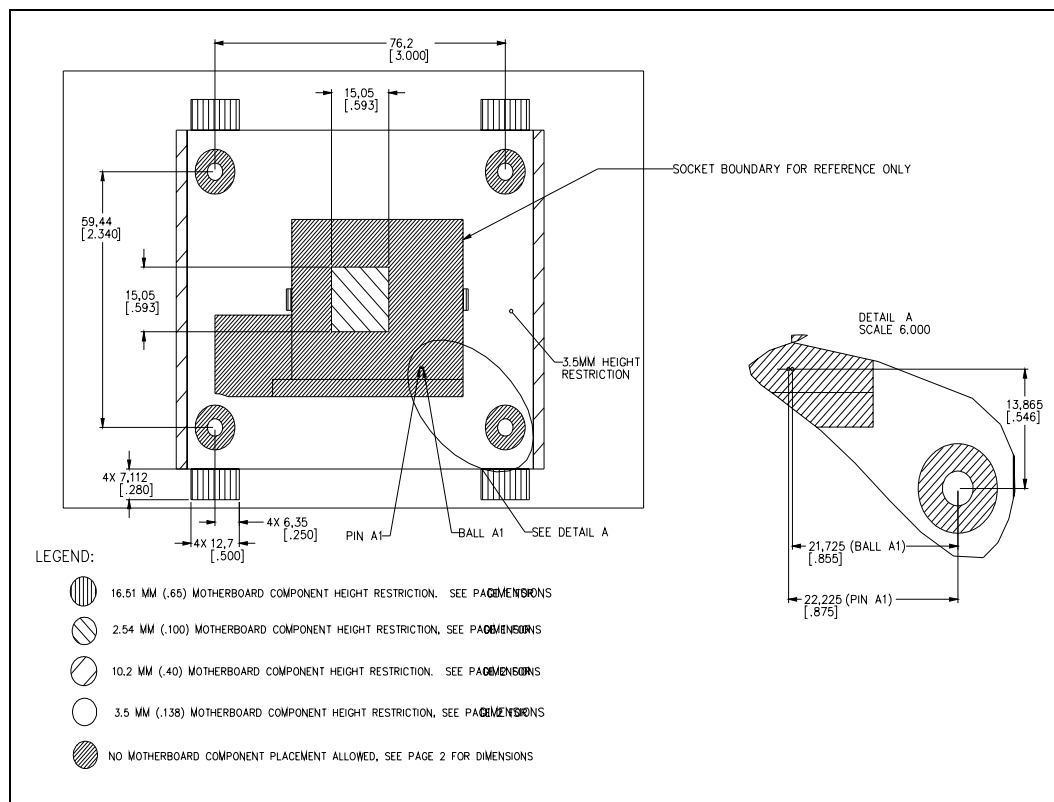
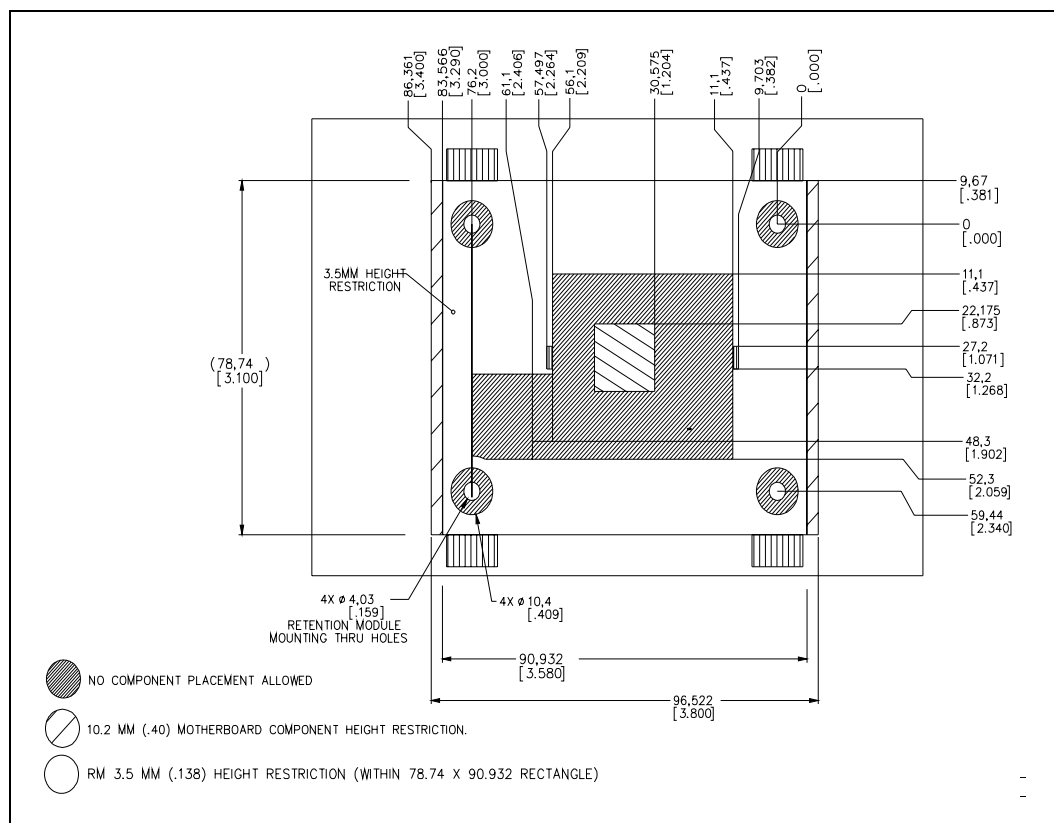


Figure 13-2. Retention Mechanism Keep-Out



Schematic Checklist

14

14.1 Processor Checklist

Table 14-1 is a schematic checklist for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments	✓
Processor / MCH Signals			
A[35:3]	• Connect to HA[35:3] pins on MCH.		
ADS#	• Connect to the associated pin on the MCH.		
ADSTB[1:0]#	• Connect to HADSTB[1:0]# pins on MCH.		
BNR#	• Connect to the associated pin on the MCH.		
BPRI#	• Connect to the associated pin on the MCH.		
BR0#	• Connect to the associated pin on the MCH. • Terminate to VCC_CPU through a 150 Ω resistor near the processor.		
RESET#	• Connect to the associated pin on the MCH. • Terminate to VCC_CPU through a 150–220 $\Omega \pm 5\%$ resistor near the processor.		
D[63:0]#	• Connect to HD[63:0]# pins on MCH.		
DBI[3:0]#	• Connect to the associated pin on the MCH.		
DBSY#	• Connect to the associated pin on the MCH.		
DEFER#	• Connect to the associated pin on the MCH.		
DRDY#	• Connect to the associated pin on the MCH.		
DSTBN[3:0]#	• Connect to HDSTBN[3:0]# pins on MCH.		
DSTBP[3:0]#	• Connect to HDSTBP[3:0]# pins on MCH.		
HIT#	• Connect to the associated pin on the MCH.		
HITM#	• Connect to the associated pin on the MCH.		
LOCK#	• Connect to HLOCK# pin on MCH.		
REQ[4:0]#	• Connect to HREQ[4:0]# pins on MCH.		
RS[2:0]#	• Connect to the associated pin on the MCH.		
TRDY#	• Connect to HTRDY# pin on MCH.		

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments	✓
Processor / Intel® ICH4 Signals			
A20M#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). 		
CPUSLP#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). 		
FERR#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4. Terminate to VCC_CPU through a $62\ \Omega \pm 5\%$ resistor near the ICH4. 		
IGNNE#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). 		
INIT#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). A voltage translator is required for FWH. Connect to Firmware Hub. 		
LINT[1:0]	<ul style="list-style-type: none"> LINT1 connects to ICH4 NMI (No extra pull-up resistors required). LINT0 connects to ICH4 INTR (No extra pull-up resistors required). 		
PWRGOOD	<ul style="list-style-type: none"> Connects to ICH4 CPUPWRGD pin (Weak external pull-up resistor required). Terminate to VCC_CPU through a $300\ \Omega \pm 5\%$ resistor. 		
SMI#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). 		
STPCLK#	<ul style="list-style-type: none"> Connect to the associated pin on the ICH4 (No extra pull-up resistors required). 		
Processor Only Signals			
AP[1:0]#	<ul style="list-style-type: none"> No Connect. 		
BCLK[1:0]	<ul style="list-style-type: none"> Connect to CK-408. Connect $20\ \Omega - 33\ \Omega$ series resistors to each clock signal. Connect a $49.9\ \Omega \pm 1\%$ shunt source termination (R_T) resistor to GND for each signal on the processor side of the series resistor (50 MB impedance). 		
BPM[5:0]#	<ul style="list-style-type: none"> These signals should be terminated with a $51\ \Omega \pm 5\%$ resistor to VCC_CPU near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
BINIT#	<ul style="list-style-type: none"> No Connect. 		
BSEL[1:0]	<ul style="list-style-type: none"> BSEL0: <ul style="list-style-type: none"> Connect to CK-408. Terminate to CK-408 3.3 V supply through a 1 kΩ resistor. BSEL1: <ul style="list-style-type: none"> No connect. 		
COMP[1:0]	<ul style="list-style-type: none"> Terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. Minimize the distance from termination resistor and processor pin. 		

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments	✓
DBR#	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
DP[3:0]#	<ul style="list-style-type: none"> No Connect. 		
IERR#	<ul style="list-style-type: none"> No Connect. 		
GTLREF3	<ul style="list-style-type: none"> Terminate to VCC_CPU through a $49.9\ \Omega \pm 1\%$ resistor. Terminate to GND through a $100\ \Omega \pm 1\%$ resistor. Should be $2/3\ VCC_CPU$. 		
GTLREF[2:0]	<ul style="list-style-type: none"> No connect. 		
ITP_CLK0	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
ITP_CLK1	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
MCERR#	<ul style="list-style-type: none"> No Connect. 		
PROCHOT#	<ul style="list-style-type: none"> No Connect. 		
RSP#	<ul style="list-style-type: none"> No Connect. 		
SKTOCC#	<ul style="list-style-type: none"> Connect to Glue Chip / Discrete Logic (If pin is used). 		
TCK	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
TDI	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
TDO	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
TESTHI	<ul style="list-style-type: none"> See Section 5.4.1.9. 		
THERMTRIP#	<ul style="list-style-type: none"> Terminate to VCC_CPU through a $62\ \Omega \pm 5\%$ resistor near the processor. 		
THERMDA	<ul style="list-style-type: none"> Connect to thermal monitor circuitry if used. 		
THERMDC	<ul style="list-style-type: none"> Connect to thermal monitor circuitry if used. 		
TMS	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
TRST#	<ul style="list-style-type: none"> Refer to the <i>ITP700 Debug Port Design Guide</i> for further information. 		
VCCA	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCC_CPU. 		
VCCIOPLL	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCC_CPU. 		
VCC_SENSE	<ul style="list-style-type: none"> Used as feedback to VR controller or leave as no connect. 		
VCCVID	<ul style="list-style-type: none"> Connect to 1.2 V linear regulator. The voltage specification for VCCVID is 1.2 V +10% / -5%. The voltage specification applies to both static and AC components for this voltage. In addition, the rising edge of the voltage must be monotonic. 		
VID[4:0]	<ul style="list-style-type: none"> Connect to VR or VRM. These signals must be pulled up to 3.3 V through 1 kΩ pull-ups. 		
VSSA	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCC_CPU. 		
VSS_SENSE	<ul style="list-style-type: none"> No Connect 		

14.2 Intel® E7205 Chipset MCH Checklist

For specific layout recommendations, refer to the appropriate section of this document.

Table 14-2. MCH Schematic Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	✓
Host Interface			
ADS# AP[1:0]# BINIT# BNR# BPRI# BREQ0# DBSY# DEFER# HA[35:3]# HD[63:0]# HADSTB[1:0]# HDSTBP[3:0]# HDSTBN[3:0]# HIT# HITM# HLOCK# HREQ[4:0]# HTRDY# DEP[3:0]# DRDY# RS[2:0]# RSP# CPURST# XERR#	<ul style="list-style-type: none"> See Processor section of this checklist. 		
DINV[3:0]#	<ul style="list-style-type: none"> Connect to Processor DBI[3:0]#. 		
Hub Interface A			
HI_A[11:0]	<ul style="list-style-type: none"> Maximum length of 20" (stripline routing). 		
PSTRBF_0 PSTRBS_0	<ul style="list-style-type: none"> Connect to Intel® ICH4. Must not have pull-up, pull-down, or series resistors. 	<ul style="list-style-type: none"> The length of each data signal must be matched within ± 0.1 of the associated HI_STRB differential pair. 	
Clocks, Reset, Miscellaneous Signals			
HCLKINP HCLKINN	<ul style="list-style-type: none"> Route to CK408 with a 49.9 Ω pull-down resistor to ground. 		
RSTIN#	<ul style="list-style-type: none"> Connect to PCIRST# output of the Intel® ICH4. 		
PRCOMP_A	<ul style="list-style-type: none"> Tie the COMP pin to a 32.4 $\Omega \pm 1\%$ Pull up to VCC. 	<ul style="list-style-type: none"> Used to calibrate the I/O Buffers. Resistive compensation is used by the ICH4 and MCH to adjust the buffer characteristics to specific board characteristic. Same compensation must be used on both ICH4 and MCH side. 	
HYRCOMP HXRCOMP	<ul style="list-style-type: none"> Tie the COMP pin to a 24.9 $\Omega \pm 1\%$ pull down resistor to ground. 	<ul style="list-style-type: none"> This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic. 	

Table 14-2. MCH Schematic Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	✓
PRCOMP_AGP0 PRCOMP_AGP1	<ul style="list-style-type: none"> Tie the COMP pin to a $43.2 \Omega \pm 1\%$ pull down resistor to ground. 	<ul style="list-style-type: none"> Resistive compensation is used by the AGP to adjust the buffer characteristics to specific board characteristics. 	
TESTSIG1 TESTSIG2	<ul style="list-style-type: none"> Can be left as No Connect. 		
TESTSIG3	<ul style="list-style-type: none"> Tie to a resistor divider with 100Ω to VSS and 49.9Ω to 1.3 V. 		
TESTSIG4	<ul style="list-style-type: none"> 24.9Ω pull-up to 1.3 V. 		
Voltage References - Power Planes			
HVREF[3:0] HAVREF[1:0] CCVREF	<ul style="list-style-type: none"> Use one dedicated voltage divider for all these signals. Decouple the voltage divider with $1 \mu\text{F}$ capacitor. 	<ul style="list-style-type: none"> To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface. 	
VREF_DDR	<ul style="list-style-type: none"> Route from VR to DIMMs and MCH. 		
PREF_A	<ul style="list-style-type: none"> Hub reference voltage = $0.350 \text{ V} \pm 1\%$. $R1 = 392 \pm 1\% \Omega$ $R2 = 499 \pm 1\% \Omega$ $R3 = 453 \pm 1\% \Omega$ $C1 = 0.1 \mu\text{F}$ $C2 = 0.01 \mu\text{F}$ 	<ul style="list-style-type: none"> HIVREF should be generated locally with a voltage divider circuit. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. Resistances shown are only suggested values to achieve proper reference voltage of 0.35 V. See latest board schematics for actual CRB implementation. 	
HXSWNG HYSWNG	<ul style="list-style-type: none"> The host compensation reference voltage can be implemented using a simple voltage divider circuit. $R1 = 150 \pm 1\%$ and $R2 = 301 \pm 1\%$ $C1 = C2 = 0.01 \mu\text{F}$ 	<ul style="list-style-type: none"> The HSWNG inputs of MCH are used provide reference voltage for the compensation logic. 	
HISWNG[B:A]	<ul style="list-style-type: none"> Hub reference swing voltage = $0.800 \text{ V} \pm 1\%$. $R6^1 = 80.6 \pm 1\% \Omega$ or $R6^2 = 226 \pm 1\%$ $R5^1 = 51.1 \pm 1\% \Omega$ or $R5^2 = 147 \pm 1\%$ $R4^1 = 40.2 \pm 1\% \Omega$ or $R4^2 = 113 \pm 1\%$ $C1 = 0.1 \mu\text{F}$ $C2 = 0.01 \mu\text{F}$ 	<ul style="list-style-type: none"> The MCH hub interfaces use a compensation voltage to control the buffer voltage characteristics. Resistances shown are only suggested values to achieve proper swing voltage of 0.8 V. See latest board schematics for actual CRB implementation. <p>NOTE: Use only resistors from group 1 or 2; do not mix values from these groups.</p>	

14.3 Intel® ICH4 Checklist

For specific layout recommendations, refer to the appropriate section of this document.

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 1 of 8)

Checklist Items	Recommendations	Comments	✓
PCI Interface			
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO0/REQA#, GPIO1/REQB# / REQ5#	<ul style="list-style-type: none"> These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5. 	<ul style="list-style-type: none"> See PCI 2.2 Component Specification for pull-up recommendations for VCC3_3 and VCC5. 	
PCIRST#	<ul style="list-style-type: none"> The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors. 	<ul style="list-style-type: none"> Improves Signal Integrity. 	
PCIGNT[4:0]#	<ul style="list-style-type: none"> No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to VCC3_3. 	<ul style="list-style-type: none"> These signals are actively driven by the Intel® ICH4. 	
PME#	<ul style="list-style-type: none"> No extra pull-up resistor. 	<ul style="list-style-type: none"> This signal has integrated pull-up of 18 kΩ to 42 kΩ. 	
GNTA# /GPIO16, GNTB/ GNT5#/ GPIO17	<ul style="list-style-type: none"> No extra pull-up needed. 	<ul style="list-style-type: none"> These signals have integrated pull-ups of 24 kΩ. GNTA has an added strap function of "top block swap". The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function. 	
IDSEL	<ul style="list-style-type: none"> The series resistor on IDSEL should be 300 Ω to 900 Ω. 	<ul style="list-style-type: none"> See Table 10-17. 	
Hub Interface			
HICOMP	<ul style="list-style-type: none"> Tie the HICOMP pin to a 43.3 $\Omega \pm 1\%$ pull-up resistor to VCC1_5. 	<ul style="list-style-type: none"> ZCOMP No longer supported. 	
HI_VSWING	<ul style="list-style-type: none"> 800 mV. 	<ul style="list-style-type: none"> See Section 7.2. 	
LAN Interface			
LAN_CLK	<ul style="list-style-type: none"> Connect to LAN_CLK on Platform LAN Connect Device. 	<ul style="list-style-type: none"> ICH4 contains integrated 100 kΩ nominal pull-down resistor on signal. 	
LAN_RXD[2:0]	<ul style="list-style-type: none"> Connect to LAN_RXD on Platform LAN Connect Device. 	<ul style="list-style-type: none"> ICH4 contains integrated 10 kΩ pull-up resistors on interface. 	
LAN_TXD[2:0], LAN_RSTSYNC	<ul style="list-style-type: none"> Connect to LAN_TXD on Platform LAN Connect Device. 		
If the LAN connect interface is not used.	<ul style="list-style-type: none"> Platform LAN connect interface can be left NC if not used. 	<ul style="list-style-type: none"> Input buffers internally terminated. 	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 2 of 8)

Checklist Items	Recommendations	Comments	✓
EEPROM Interface			
EE_DOUT	<ul style="list-style-type: none"> Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector. 	<ul style="list-style-type: none"> ICH4 contains integrated pull-up resistor for this signal. Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH4 perspective). 	
EE_DIN	<ul style="list-style-type: none"> No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector. 	<ul style="list-style-type: none"> ICH4 contains integrated pull-up resistor for this signal. Connected to EEPROM data output signal (Output from EEPROM perspective and input from ICH4 perspective). 	
FWH/LPC Interface			
FWH[3:0] / LAD[3:0], LDRQ[1:0]	<ul style="list-style-type: none"> No extra pull-ups required. Connect straight to FWH/LPC. 	<ul style="list-style-type: none"> ICH4 Integrates 24 kΩ pull-up resistors on these signal lines. 	
FWH Decoupling	<ul style="list-style-type: none"> Follow vendor recommendation. 		
Interrupt Interface			
PIRQ[D:A]#	<ul style="list-style-type: none"> These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3. 	<ul style="list-style-type: none"> The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. 	
PIRQ[H:E]#/GPIO[5:2]	<ul style="list-style-type: none"> These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3. 	<ul style="list-style-type: none"> The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. 	
APIC	<ul style="list-style-type: none"> The APICCLK should be tied directly to GND. Pull APICD[1:0] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10 kΩ pull-down resistors). 		
SERIRQ	<ul style="list-style-type: none"> External weak (8.2 kΩ) pull-up resistor to VCC3_3 is recommended. 	<ul style="list-style-type: none"> Open drain signal. 	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 3 of 8)

Checklist Items	Recommendations	Comments	✓
GPIO			
GPIO Pins	<p>GPIO[7:0]:</p> <ul style="list-style-type: none"> • These pins are in the main power well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO1 can be used as PCI REQ5#. • GPIO[5:2] can be used as PIRQ[H:E]#. • GPIO6. • These signals are 5 V tolerant. • These pins are inputs. <p>GPIO8 and [13:11]:</p> <ul style="list-style-type: none"> • These pins are in the resume power well. Pull-ups must use the VccSus3_3 plane. • Unused resume well inputs must be pulled up to VccSus3_3. • These signals are not 5 V tolerant. • GPIO11 can be used as SMBALERT#. • These pins are inputs. <p>GPIO[23:16]:</p> <ul style="list-style-type: none"> • Fixed as output only. Can be left NC. • GPIO22 is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO17 can be used as PCI GNT5#. • GPIO18. • GPIO19. • GPIO20. • GPIO21. • GPIO22 (open drain). • GPIO23. • These signals are not 5 V tolerant. <p>GPIO[28, 27, 25, 24]:</p> <ul style="list-style-type: none"> • I/O pins. Default as outputs so can be left as NC. • These pins are in the Resume Power Well. • GPIO[28:27, 25] From resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled-up). • GPIO24. • These signals are not 5 V tolerant. <p>GPIO[43:32]:</p> <ul style="list-style-type: none"> • I/O pins. From main power well. • Default as outputs. • These signals are not 5 V tolerant. 	<ul style="list-style-type: none"> • Ensure that ALL unconnected signals are OUTPUTS ONLY! 	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 4 of 8)

Checklist Items	Recommendations	Comments	✓
USB			
USBRBIAS	<ul style="list-style-type: none"> 22.6 $\Omega \pm 1\%$ connected to ground. 		
USBRBIAS#	<ul style="list-style-type: none"> Connected to the same 22.6 $\Omega \pm 1\%$ resistor to ground as USBRBIAS. 		
USBP[5:0]P, USBP[5:0]N	<ul style="list-style-type: none"> No external resistors required. 	<ul style="list-style-type: none"> Output driver impedance of 45 Ω provided. 	
OC[5:0]	<ul style="list-style-type: none"> If not used, use 10 kΩ to VccSus3_3. 	<ul style="list-style-type: none"> Inputs must not float. 	
Unconnected USB data signals	<ul style="list-style-type: none"> Unconnected USB data signals can be left as no-connects. 		
Power Management			
THRM#	<ul style="list-style-type: none"> Connect to temperature Sensor. pull-up if not used (an 8.2 kΩ pull-up resistor to VCC3_3). 	<ul style="list-style-type: none"> Input to ICH4 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up. 	
THRMTRIP#	<ul style="list-style-type: none"> See Section 5.4.1.1 	<ul style="list-style-type: none"> Input to Intel ICH4 cannot float. 	
SLP_S3#, SLP_S4# SLP_S5#	<ul style="list-style-type: none"> No pull-up/down resistors needed. Signals driven by ICH4. 	<ul style="list-style-type: none"> Signals driven by ICH4. 	
PWROK	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_5 have reached their nominal voltages. 	<ul style="list-style-type: none"> Timing requirement. 	
PWRBTN#	<ul style="list-style-type: none"> No extra pull-up resistors. 	<ul style="list-style-type: none"> This signal has an integrated pull-up of 18 kΩ – 42 kΩ. 	
SYS_RESET#	<ul style="list-style-type: none"> Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also a (100 Ω to 8.2 kΩ) pull-down resistor isolated from SYS_RESET# by means of a normally open switch. 	<ul style="list-style-type: none"> Input to Intel ICH4 cannot float. This pin forces an internal reset to the ICH4 after the signal is internally debounced. 	
RI#	<ul style="list-style-type: none"> RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well. 	<ul style="list-style-type: none"> If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event. 	
RSMRST#	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#. 	<ul style="list-style-type: none"> Timing requirement. 	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 5 of 8)

Checklist Items	Recommendations	Comments	✓
LAN_RST#	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#. 	<ul style="list-style-type: none"> Timing requirement. 	
Processor Signals			
A20M#, CPU_SLP#, IGNNE#, INTR, NMI, SMI#, STPCLK#	<ul style="list-style-type: none"> Point-to-point connection. No external termination required at the ICH4. See Section 5.4.1.2 for processor guidelines. 		
INIT#	<ul style="list-style-type: none"> See Section 5.4.1.3 and Section 10.4.4. 		
FERR#	<ul style="list-style-type: none"> Requires external pull-up resistor to CPUVDD. See Section 5.4.1.1 for processor guidelines. 		
RCIN#, A20GATE	<ul style="list-style-type: none"> Pull-up signals to VCC3_3 through a 10 kΩ resistor. 	<ul style="list-style-type: none"> Typically driven by open drain external micro-controller. 	
CPUPWRGD	<ul style="list-style-type: none"> Connect to the processor's CPUPWRGD input. Requires external pull-up resistor. See Section 14.1 for processor guidelines. 	<ul style="list-style-type: none"> Refer to documentation of the processor that platform utilizes for specific values. This signal represents a logical AND of the Intel ICH4's PWROK and VRMPWRGD signals. 	
System Management			
SMBDATA, SMBCLK	<ul style="list-style-type: none"> Require external pull-up resistors. See Section 10.3.9 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination). Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1. 	<ul style="list-style-type: none"> Value of pull-ups resistors determined by line load. 	
SMBALERT# / GPIO11	<ul style="list-style-type: none"> See GPIO section if SMBALERT# not implemented. 		

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 6 of 8)

Checklist Items	Recommendations	Comments	✓
SMLINK[1:0]	<ul style="list-style-type: none"> Requires external pull-up resistors. See Section 10.3.9 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination). Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1. 	<ul style="list-style-type: none"> Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ. 	
INTRUDER#	<ul style="list-style-type: none"> Pull signal to VccRTC (VBAT) through ~10 kΩ. 	<ul style="list-style-type: none"> Signal in VccRTC (VBAT) well. 	
RTC			
VBIAS	<ul style="list-style-type: none"> The VBIAS pin of the ICH4 is connected to a 0.047 μF capacitor. See Figure 10-32. 	<ul style="list-style-type: none"> For noise immunity on VBIAS signal. 	
RTCX1,RTCX2	<ul style="list-style-type: none"> Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor. See Section 10.3.11.3 for capacitor guidelines. 	<ul style="list-style-type: none"> The external circuitry shown in Figure 10-32 will be required to maintain the accuracy of the RTC. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VccRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds. 	
RTCRST#	<ul style="list-style-type: none"> Time constant due to RC filter on this line should be 18-25 ms. Recommended value for Resistor = 180 kΩ and Capacitor is 0.1 μF. 	<ul style="list-style-type: none"> Timing Requirement. 	
AC'97			
AC_SDOOUT	<ul style="list-style-type: none"> Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. Series termination resistor 0 Ω to 47 Ω on board codec. 	<ul style="list-style-type: none"> This pin has a weak internal 20 kΩ nominal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down. 	
AC_SDIN1, AC_SDIN0	<ul style="list-style-type: none"> Internal pull-downs in Intel ICH4; no external pull-downs required. Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4. 	<ul style="list-style-type: none"> These pins have a weak internal 20 kΩ nominal pull-down. 	
AC_SDIN2	<ul style="list-style-type: none"> Series termination resistor 33 Ω to 47 Ω from the AC_SDIN lines to the ICH4. 	<ul style="list-style-type: none"> This pin has a weak internal 20 kΩ nominal pull-down. 	
AC_BITCLK	<ul style="list-style-type: none"> No extra pull-down resistors required. Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4. 	<ul style="list-style-type: none"> This pin has a weak internal 20 kΩ nominal pull-down. 	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 7 of 8)

Checklist Items	Recommendations	Comments	✓
AC_SYNC	<ul style="list-style-type: none"> No extra pull-down resistors required. 	<ul style="list-style-type: none"> Some implementations add termination for signal integrity. Platform specific. 	
Miscellaneous Signals			
SPKR	<ul style="list-style-type: none"> See Section 10.3.5.3. 	<ul style="list-style-type: none"> Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled. 	
TP0	<ul style="list-style-type: none"> TP0 requires external pull-up resistor to VccSus3_3. 		
Power			
V_CPU_IO[2:0]	<ul style="list-style-type: none"> The power pins should be connected to the proper power plane for the processor's CMOS compatibility signals. Use one 0.1 μF decoupling capacitor. 	<ul style="list-style-type: none"> Used to pull-up all processor interface signals. 	
VccRTC	<ul style="list-style-type: none"> Use one 0.1 μF decoupling capacitor. No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for clear CMOS. 		
VCC3_3	<ul style="list-style-type: none"> Use six 0.1 μF decoupling capacitors. 		
VccSus3_3	<ul style="list-style-type: none"> Use two 0.1 μF decoupling capacitors. 		
VCC1_5	<ul style="list-style-type: none"> Use two 0.1 μF decoupling capacitors. 		
VccSus1_5	<ul style="list-style-type: none"> Use two 0.1 μF decoupling capacitor. 		
V5REF_Sus	<ul style="list-style-type: none"> Use one 0.1 μF decoupling capacitor. V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5REF_Sus. 		
V5REF	<ul style="list-style-type: none"> Use one 0.1 μF decoupling capacitor. V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. 		
VCCPLL	<ul style="list-style-type: none"> Use one 0.1 μF decoupling capacitor and one 0.01 μF decoupling capacitor. 		
VCCHI	<ul style="list-style-type: none"> Use two 0.1 μF capacitors. 		
HIREF	<ul style="list-style-type: none"> 350 mV. 		

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 8 of 8)

Checklist Items	Recommendations	Comments	✓
IDE Checklist			
PDD[15:0], SDD[15:0]	<ul style="list-style-type: none"> No extra series termination resistors or other pull-ups/pull-downs are required. PDD7/SDD7 does not require a 10 kΩ pull-down resistor. Refer to ATA ATPI-6 Specification. 	<ul style="list-style-type: none"> These signals have integrated series resistors. <p>NOTE: Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.</p>	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	<ul style="list-style-type: none"> No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. 	<ul style="list-style-type: none"> These signals have integrated series resistors. <p>NOTE: Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.</p>	
PDREQ, SDREQ	<ul style="list-style-type: none"> No extra series termination resistors. No pull-down resistors needed. 	<ul style="list-style-type: none"> These signals have integrated series resistors in the ICH4. 	
PIORDY, SIORDY	<ul style="list-style-type: none"> No extra series termination resistors. Pull-up to VCC3_3 via a 4.7 kΩ resistor. 	<ul style="list-style-type: none"> These signals have integrated series resistors in the ICH4. 	
IRQ14, IRQ15	<ul style="list-style-type: none"> Recommend 8.2 kΩ –10 kΩ pull-up resistors to VCC3_3. No extra series termination resistors. 	<ul style="list-style-type: none"> Open drain outputs from drive. 	
IDERST#	<ul style="list-style-type: none"> The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal. 		
Cable Detect	<p>Host Side/Device Side Detection (<i>recommended method</i>):</p> <ul style="list-style-type: none"> Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. <p>Device side detection:</p> <ul style="list-style-type: none"> Connect a 0.047 μF capacitor from IDE pin PDIAG#/CBLID to GND. No ICH4 connection. 	<ul style="list-style-type: none"> The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. <p>NOTE: All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables.</p>	

14.4 Hub Interface Checklist

Table 14-4. Hub Interface Checklist

Checklist Items	Recommendations	Comments	✓
MCH / Intel® ICH4 Signals			
HI_x[11:0]	<ul style="list-style-type: none"> Connect together. 		
HI_STB	<ul style="list-style-type: none"> Connect together. 		
HI_STB#	<ul style="list-style-type: none"> Connect together. 		
HI_REF	<ul style="list-style-type: none"> Connect voltage divider circuit with $R1=R2=150\ \Omega \pm 1\%$. Use two 0.1 μF capacitors within 150 mils of the ICH4. The MCH should be decoupled with one 0.1 μF capacitor within 150 mils of the package and one 10 μF capacitor nearby. Bypass to GND through a 0.1 μF capacitor located near each component's (MCH and ICH4) HIREF pin. Decouple with a 0.1 μF capacitor placed near the divider circuit. 		
VCC1_8	<ul style="list-style-type: none"> Connect to 1.8 V power supply. 		
MCH Signals Only			
PRCOMP_A	<ul style="list-style-type: none"> Pull-up to VCC1_3 through a $32.4\ \Omega \pm 1\%$ resistor. 		
ICH4 Signals Only			
HICOMP	<ul style="list-style-type: none"> Tie the HICOMP pin to a $43.3\ \Omega \pm 1\%$ pull-up resistor to VCC1_5. ZCOMP is no longer supported. 		

14.5 DDR SDRAM Checklist

Table 14-5. DDR SDRAM Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	✓
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	<ul style="list-style-type: none"> Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 39 Ω resistor. Resistor packs can be used, but do not use address/command or control signals on the same RPACK as these signals. 		
DQS[17:9]	<ul style="list-style-type: none"> These signals are left floating at the MCH. Ground them at the DIMM. 		
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	<ul style="list-style-type: none"> Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Resistor packs can be used, but do not use data/strobe or control signals on the same RPACK as these signals. 		
CS_x[3:0]# CKE_x[3:0]	<ul style="list-style-type: none"> Connect to a single DIMM, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Refer to Table 6-2 for correct DIMM pin mapping. Resistor packs can be used, but don't use data/strobe or address/command signals on the same RPACK as these signals. 		
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	<ul style="list-style-type: none"> Route each signal and its complement differentially to the DIMM. Signal does not route to termination. Refer to Table 6-5 for correct DIMM pin mapping. 		
VREF	<ul style="list-style-type: none"> Connect to a resistor divider, 49.9 Ω to both 2.5 V and GND near the MCH, and add a 1 μF decoupling capacitor from VREF to ground near the divider. Connect to the VREF pin on each DIMM in the channel. Decouple each DIMM with a 0.1 μF capacitor. Decouple with a 0.1 μF capacitor near the MCH. See Section 6.4.4 for details. 		
MCH Signals Only			
CMDCLK_x[3:2] CMDCLK_x[3:2]#	<ul style="list-style-type: none"> These signals are left floating at the MCH. 		
RCVENOUT_x#	<ul style="list-style-type: none"> Connect to a resistor divider, 78.7 Ω to both 2.5 V and ground. 		
DRCOMPVREF_H DRCOMPVREF_V	<ul style="list-style-type: none"> Connect these signals together and to a resistor divider, 49.9 Ω to both 2.5 V and ground, decoupled with a 100 pF capacitor from DRCOMPVREF to ground. 		
DRCOMP_H DRCOMP_V	<ul style="list-style-type: none"> Connect to ground through a 24.9 Ω resistor. 		
DDR_STRAP	<ul style="list-style-type: none"> Connect directly to 2.5 V. 		
ODTCOMP	<ul style="list-style-type: none"> Connect to ground through a 402 Ω resistor. 		
VCCDDR	<ul style="list-style-type: none"> Connect to 2.5 V. 		

Table 14-5. DDR SDRAM Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	✓
DIMM Signals Only			
A13 FETEN VDDID	<ul style="list-style-type: none"> No Connect. 		
SDA	<ul style="list-style-type: none"> Connect to SMBus Data. 		
SCL	<ul style="list-style-type: none"> Connect to SMBus Clock. 		
VDD VDDQ	<ul style="list-style-type: none"> Connect to 2.5 V. 		
VSS	<ul style="list-style-type: none"> Connect to ground. 		
VDDSPD	<ul style="list-style-type: none"> Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V Strongly recommended connecting to 3.3 V. 		
Decoupling Capacitors			
MCH High-Frequency Decoupling	<ul style="list-style-type: none"> Place ten 0603 0.1 μF MLC capacitors near the MCH. Connect from 2.5 V to ground. 		
MCH Bulk Decoupling	<ul style="list-style-type: none"> Place four 100 μF capacitors between the MCH and the first DIMM. Connect from 2.5 V to ground. 		
DIMM Decoupling	<ul style="list-style-type: none"> Place two 100 μF capacitors per DIMM, one each on either side of the DIMM socket. Connect from 2.5 V to ground. 		
VTT Decoupling	<ul style="list-style-type: none"> Place one 0.1 μF capacitor for every two termination resistors (or 2 caps/RPACK). Place four 4.7 μF capacitors around the termination island, two on either side (See Figure 6-30). Connect from 1.25 V to ground. 		

14.6 AGP Interface Checklist

Table 14-6. AGP Interface Checklist (Sheet 1 of 2)

Checklist Items ¹	Recommendations	Comments	✓
MCH / Connector Signals			
AD_STB[1:0] (AGP 2.0) AD_STBF[1:0] (AGP 3.0)	<ul style="list-style-type: none"> Connect to AGP connector. 		
AD_STB[1:0]# (AGP 2.0)/ AD_STBS[1:0] (AGP 3.0)			
DBI_LO (AGP 3.0)			
GAD[31:0]			
GC/BE[3:0]# (AGP 2.0)/ GC#/BE[3:0] (AGP 3.0)			
GC_DET#	<ul style="list-style-type: none"> See Figure 9-1 		
GDEVSEL# (AGP 2.0)/ GDEVSEL (AGP 3.0)	<ul style="list-style-type: none"> Connect to AGP connector. 		
GFRAME# (AGP 2.0)/ GFRAME (AGP 3.0)			
GGNT# (AGP 2.0)/ GGNT (AGP 3.0)			
GIRDY# (AGP 2.0)/ GIRDY (AGP 3.0)			
GPAR			
GREQ# (AGP 2.0) GREQ (AGP 3.0)			
GSTOP# (AGP 2.0)/ GSTOP (AGP 3.0)			
GTRDY# (AGP 2.0)/ GTRDY (AGP 3.0)			
MB_DET#	<ul style="list-style-type: none"> Terminate to GND. 		
PIPE# (AGP 2.0)/ DBI_HI (AGP 3.0)	<ul style="list-style-type: none"> Connect to AGP connector. 		
RBF (AGP 2.0)/ RBF# (AGP 3.0)			
SBA[7:0] (AGP 2.0)/ SBA[7:0]# (AGP 3.0)			
SB_STB (AGP 2.0)/ SB_STBF (AGP 3.0)			
SB_STB# (AGP 2.0)/ SB_STBS (AGP 3.0)			
ST0			
ST1			
ST2			
WBF# (AGP 2.0)/ WBF (AGP 3.0)			
VCC1_5	<ul style="list-style-type: none"> Connect to 1.5 V power supply. 		

Table 14-6. AGP Interface Checklist (Sheet 2 of 2)

Checklist Items ¹	Recommendations	Comments	✓
Connector Signals Only			
3.3Vaux	• Connect to PCI 3.3VAUX.		
12V	• Connect to 12 V.		
AGPCLK	• Connect to CK408.		
INTA#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document.		
INTB#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document.		
PERR	• Refer to Section 9.3.1 .		
SERR# (AGP 2.0)/ SERR (AGP 3.0)	• Connect to AGP connector.		
OVRcnt	• No connect.		
PCIRST	• Connect to PCI slot PCIRST.		
PME#	• Connect to PCI PME#.		
TYPEDET#	• Refer to Section 9.3.2 .		
USB+	• No connect.		
USB-	• No connect.		
VCC	• Connect to VCC3_3.		
VCC5	• Connect to VCC.		
VDDQ	• Connect to V1.5CORE.		
PREF_AGP[1:0]	• Connect to VREF divider network at the AGP connector.		
MCH Signals Only			
PREF_AGP[1:0]	<ul style="list-style-type: none"> • Connect to VREFCG pin on connector. • Terminate to ground through a 0.1 μF capacitor at the MCH. 		
PRCOMP_AGP[1:0]	• Pull each signal to VCC_AGP through a 43.2 $\Omega \pm 1\%$ resistor.		

NOTE:

1. Checklist items may have differing names depending on the AGP signaling mode being used. In these cases, the differing names are separated by a slash with AGP2.0 signal names listed first, followed by AGP3.0 signal names.

14.7 CK 408 Clock Interface Checklist

Table 14-7. CK 408 Clock Interface Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	✓
66BUFF0	<ul style="list-style-type: none"> Connect to MCH. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
66BUFF1	<ul style="list-style-type: none"> Connect to ICH4. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
66BUFF2	<ul style="list-style-type: none"> Connect to AGP. Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
66IN	<ul style="list-style-type: none"> No Connect. 		
CPU[1:0]	<ul style="list-style-type: none"> Connect to processor. Connect to a series $27\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. 		
CPU[1:0]#	<ul style="list-style-type: none"> Connect to processor. Connect to a series $27\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. 		
CPU2 CPU2#	<ul style="list-style-type: none"> Connect to MCH. Connect to a series $27\ \Omega \pm 5\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor. 		
CPU_STOP#	<ul style="list-style-type: none"> Terminate to VCC3_3 through a $1\ \text{k}\Omega \pm 1\%$ resistor. 		
DOT48MHz	<ul style="list-style-type: none"> No Connect. 		
IREF	<ul style="list-style-type: none"> Terminate to GND through a $475\ \Omega \pm 1\%$ resistor. 		
MULT0	<ul style="list-style-type: none"> Connected from the VCC3_3 through a series $10\ \text{k}\Omega \pm 5\%$ resistor and terminate to GND through a parallel $1\ \text{k}\Omega \pm 1\%$ resistor. 		
PCI[6:0]	<ul style="list-style-type: none"> Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
PCIF[2:0]	<ul style="list-style-type: none"> Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
PCI_STOP#	<ul style="list-style-type: none"> Terminate to VCC3_3 through a $1\ \text{k}\Omega \pm 1\%$ resistor. 		
PWRDWN#	<ul style="list-style-type: none"> Terminate to VCC3_3 through a $1\ \text{k}\Omega \pm 1\%$ resistor. 		
REF0	<ul style="list-style-type: none"> Connect to a series $33\ \Omega \pm 5\%$ resistor and terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
S[1:0]	<ul style="list-style-type: none"> Terminate to VCC_CLK through a $1\ \text{k}\Omega \pm 5\%$ resistor. 		
S2	<ul style="list-style-type: none"> Terminate to GND through a $1\ \text{k}\Omega \pm 5\%$ resistor. 		
SCLK	<ul style="list-style-type: none"> Connect to DIMMs. 		
SDATA	<ul style="list-style-type: none"> Connect to DIMMs. 		
USB48MHz	<ul style="list-style-type: none"> Connect to ICH4. Terminate to GND through a $33\ \Omega \pm 5\%$ resistor and a $10\ \text{pF} \pm 5\%$ capacitor. 		
VDD	<ul style="list-style-type: none"> Terminate to VCC_CLK. 		

Table 14-7. CK 408 Clock Interface Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	✓
VDD48MHz	<ul style="list-style-type: none"> • Terminate to VCC_CLK. 		
VDDA	<ul style="list-style-type: none"> • Terminate to GND through a $0.1\ \mu\text{F} \pm 5\%$ capacitor. 		
VSS	<ul style="list-style-type: none"> • Terminate to GND. 		
VSSA	<ul style="list-style-type: none"> • Terminate to GND. 		
VSS48MHz	<ul style="list-style-type: none"> • Terminate to GND. 		
VSSIREF	<ul style="list-style-type: none"> • Terminate to GND. 		
VTT_PWRGD#	<ul style="list-style-type: none"> • Connect to an inverted copy of VCC_CPU. Refer to the respective section of the design guide for more details. 		
XTAL_IN	<ul style="list-style-type: none"> • Terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		
XTAL_OUT	<ul style="list-style-type: none"> • Terminate to GND through a $10\ \text{pF} \pm 5\%$ capacitor. 		

Layout Checklist

15

15.1 System Bus Layout Checklist

Table 15-1. System Bus Layout Checklist (Sheet 1 of 2)

No.	Recommendations	Comments	✓
Data Signals: D[63:0]#, DBI[3:0]#			
1	• Point-to-point Topology.		
2	• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.		
3	• 2.0 inches to 10.0 inches pin-to-pin data signal lengths.		
4	• Traces should be 7 mils wide with 13 mil spacing.		
5	• Data signals of the same source synchronous group should be routed to the same pad-to-pad length within +100 mils of the associated strobes.		
Data Strokes: DSTBN/P[3:0]			
1	• Traces should be 7 mils wide with 13 mil spacing.		
2	• Data strobes and their compliments should be routed within +25 mils of the same pad to pad length.		
Address Strokes: ADSTB[1:0]			
1	• Point-to-point Topology.		
2	• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.		
3	• 2.0 inches to 10.0 inches pin-to-pin address signal lengths.		
4	• Traces should be 7 mils wide with 13 mil spacing.		
Address Signals: A[3:31]#, REQ[4:0]			
1	• Traces should be 7 mils wide with 13 mil spacing.		
2	• 2.0 inches to 10.0 inches pin-to-pin address signal lengths.		
3	• Address signals of the same source synchronous group should be routed to the same pad-to-pad length within +200 mils of the associated strobes.		
Clocks: HCLKINP/HCLKINN			
1	• These should be routed as a differential pair with 7 mil traces and 7 mil spacing between them.		
2	• 2.5 inches to 10.0 inches pin-to-pin common clock lengths.		
3	• 25 mil spacing should be maintained around all clocks.		

Table 15-1. System Bus Layout Checklist (Sheet 2 of 2)

No.	Recommendations	Comments	✓
Processor AGTL+: FERR#, PROCHOT#, THERMTRIP#			
1	• Traces should be 5 mils wide with 7 mil spacing.		
2	• 1.0 inches to 12.0 inches max from Processor to Intel® ICH4.		
3	• 3.0 inches max from ICH4 to VDD.		
ICH4 AGTL+: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK			
1	• Traces should be 5 mils wide with 7 mil spacing.		
2	• 12.0 inches max from ICH4 to Processor.		
3	• Level shifting is required from the INIT# pin to FWH.		
ICH4 Open Drain AGTL+: PWRGOOD			
1	• 7 mil spacing.		
2	• 1.0 inch to 12.0 inches max from ICH4 to Processor.		
3	• 1.1 inches max breakout length.		
4	• 3.0 inches max from Processor to VDD.		
Miscellaneous AGTL+: BR0#, RESET#			
1	• Terminate using discrete components on the system board.		
2	• Minimize the distance between the terminating resistors and processor.		
3	• Connect the signals between these components.		
Miscellaneous AGTL+: COMP[1:0]			
1	• Minimize the distance from terminating resistor.		
Miscellaneous AGTL+: THERMDA, THERMDC			
1	• 10 mils wide by 10 mil spacing.		
2	• Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 inches to 8.0 inches away as long as the worst noise sources such as clock generators, data, buses and address buses, etc. are avoided.		
3	• Route in parallel and close together with ground guards enclosed.		

15.2 Intel® ICH4 Layout Checklist

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 1 of 5)

No.	Recommendations	Comments	✓
1	• Board impedance must be 50 Ω \pm 10% if using Hub Interface 1.5.		
2	• Traces must be routed 5 mils wide with 15 mils spacing.		
3	• To breakout of the MCH and Intel® ICH4 package, the Hub Interface signals can be routed 5 on 5. Signals must be separated to 5 on 15 within 300 mils of the package.		
4	• Max trace length 20" is dependant on MCH/ICH4 simulations.		
5	• Data signals must be matched within \pm 0.1 inches of the HI_STB differential pair.		
6	• HI_STB/HI_STBS and HI_STB#/HI_STBF lengths must be matched.		
7	• (Local Reference Divider Circuit only) HIREF dividers should be placed no more than 4 inches of away from MCH or ICH4.		
8	• HI signals must be referenced to ground.		
IDE Interface			
1	• 5 mil wide and 7 mil spaces.		
2	• Max trace length is 8 inches long.		
3	• The maximum length difference between the data and strobe lengths is 0.5 inches.		
USB 2.0			
1	• With minimum trace lengths, route high-speed clock and USB differential pairs first.		
2	• Route USB signals ground referenced.		
3	• Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.		
4	• When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.		
5	• Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.		
6	• Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 2 of 5)

No.	Recommendations	Comments	✓
7	<ul style="list-style-type: none"> Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) 		
8	<ul style="list-style-type: none"> Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out. 		
9	<ul style="list-style-type: none"> Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB. 		
10	<ul style="list-style-type: none"> Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: 7.5 on 7.5 spacing with 4-layer, 4.3 mil prepreg stackup). 		
11	<ul style="list-style-type: none"> Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils. 		
12	<ul style="list-style-type: none"> Use 20 mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. 		
13	<ul style="list-style-type: none"> USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils. 		
14	<ul style="list-style-type: none"> No termination resistors needed for USB. 		
15	<ul style="list-style-type: none"> USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 Ω 1% resistor to ground. 		
16	<ul style="list-style-type: none"> Maximum length from the ICH4 to the back panel should not be greater than 17 inches. Maximum length from the ICH4 to the CNR should not be greater than 8 inches. 		
Platform LAN Connect Interface			
1	<ul style="list-style-type: none"> Trace spacing: 5 mils wide, 10 mil. 		
2	<ul style="list-style-type: none"> Stubs due to R-pak CNR/LOM stuffing option should not be present. 	<ul style="list-style-type: none"> To minimize inductance. 	
3	<ul style="list-style-type: none"> Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace). 	<ul style="list-style-type: none"> To meet timing and signal quality requirements. 	
4	<ul style="list-style-type: none"> Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY. 	<ul style="list-style-type: none"> To meet timing and signal quality requirements. 	
5	<ul style="list-style-type: none"> Keep the total length of each differential pair (from PHY to connector) under 4 inches (preferably less than 2 inches). 	<ul style="list-style-type: none"> Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER. 	

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 3 of 5)

No.	Recommendations	Comments	✓
6	<ul style="list-style-type: none"> Do not route the transmit differential traces closer than 100 mils to the receive differential traces. 	<ul style="list-style-type: none"> To minimize crosstalk. 	
7	<ul style="list-style-type: none"> Distance between differential traces and any other signal line is 100 mils. (300 mils recommended). 	<ul style="list-style-type: none"> To minimize crosstalk. 	
8	<ul style="list-style-type: none"> Route 5 mils on 10 mils for differential pairs (out of LAN phy). 	<ul style="list-style-type: none"> To meet timing and signal quality requirements. 	
9	<ul style="list-style-type: none"> Differential trace impedance should be controlled to be ~100 Ω. 	<ul style="list-style-type: none"> To meet timing and signal quality requirements. 	
10	<ul style="list-style-type: none"> For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends. 	<ul style="list-style-type: none"> To meet timing and signal quality requirements. 	
11	<ul style="list-style-type: none"> Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. 	<ul style="list-style-type: none"> This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards. 	
12	<ul style="list-style-type: none"> Do not route traces and vias under crystals or oscillators. 	<ul style="list-style-type: none"> This will prevent coupling to or from the clock. 	
13	<ul style="list-style-type: none"> Trace width to height ratio above the ground plane should be between 1:1 and 3:1. 	<ul style="list-style-type: none"> To control trace EMI radiation. 	
14	<ul style="list-style-type: none"> Traces between decoupling and I/O filter capacitors should be as short and wide as practical. 	<ul style="list-style-type: none"> Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors. 	
15	<ul style="list-style-type: none"> Vias to decoupling capacitors should be sufficiently large in diameter. 	<ul style="list-style-type: none"> To decrease series inductance. 	
16	<ul style="list-style-type: none"> Avoid routing high-speed LAN near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices. 	<ul style="list-style-type: none"> To minimize crosstalk. 	
17	<ul style="list-style-type: none"> Isolate I/O signals from high-speed signals. 	<ul style="list-style-type: none"> To minimize crosstalk. 	
18	<ul style="list-style-type: none"> Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge. 	<ul style="list-style-type: none"> This minimizes the potential for EMI radiation problems. 	
19	<ul style="list-style-type: none"> Place at least one bulk capacitor (4.7 μF or greater OK) on each side of the Intel® 82562ET/EM. 	<ul style="list-style-type: none"> Research and development has shown that this is a robust design recommendation. 	
20	<ul style="list-style-type: none"> Place decoupling capacitors (0.1 μF) as close to the Intel® 82562ET/EM as possible. 		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 4 of 5)

No.	Recommendations	Comments	✓
AC'97			
1	Z_O AC97 = $60 \Omega \pm 15\%$.		
2	4 mil trace width, 6 mil spacing between traces.		
3	AC_SDIN Max Trace Lengths <ul style="list-style-type: none"> • ICH4 to primary codec: L = 14 inches. • From Primary Codec T junction to CNR: L = 6 inches. • CNR: L = 14 inches. (Using given example 4-layer 4.3 mil prepreg stackup.) 		
4	AC_SDOOUT Max Trace Lengths <ul style="list-style-type: none"> • ICH4 to primary codec: L = 14 inches. • CNR: L = 14 inches. (Using given example 4-layer 4.3 mil prepreg stackup.) 		
5	AC_BIT_CLK Max Trace Lengths <ul style="list-style-type: none"> • ICH4 to primary codec: L = 13.6 inches. • CNR: L = 13.6 inches. (Using given example 4-layer 4.3 mil prepreg stackup.) 		
6	<ul style="list-style-type: none"> • Series termination resistor on AC_BIT_CLK line should be no more than 0.9 to 7.6 inches from the ICH4. 		
7	<ul style="list-style-type: none"> • Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the CNR card or the on board codec. 		
Clocking			
1	<ul style="list-style-type: none"> • CLK_33 goes to ICH4, FWH, and SIO. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 15 inches max. Routed on one Layer. 		
2	<ul style="list-style-type: none"> • PCI_33 goes to PCI Device or PCI Slot, there are 5 clocks. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 13 inches max. Routed on one Layer. 		
3	<ul style="list-style-type: none"> • CLK_66 goes to ICH4 and MCH. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 14 inches max. Routed on one Layer. 		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 5 of 5)

No.	Recommendations	Comments	✓
RTC			
1	• RTC LEAD length = 1.0 inches Max.		
2	• Minimize capacitance between RTCX1 and RTCX2.		
3	• Put GND plane underneath Crystal components.		
4	• Do not route switching signals under the external components (unless on other side of board).		
5	• If SUSCLK is not used in the platform it should be routed to a testpoint.	• The ability to probe this signal can decrease the resolution time for RTC related issues.	
PCI Guidelines			
1	• Data Lines - See specific topology guidelines in Table 10-17).		
2	• Clock Lines (See Figure 10-29 and Table 10-18).		
3	• IDSEL (See Figure 10-28).		
Processor CMOS Guidelines			
1	• Series termination should be less than 2000 mils from the ICH4. Total length from the ICH4 to the processor should be no more than 19 inches.		
FWH Decoupling Guidelines			
1	• 0.1 μ F capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		
2	• 4.7 μ F capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		

15.2.1 Intel® ICH4 Decoupling

Table 15-3. Intel® Decoupling Checklist

No.	Recommendations	Comments	✓
1	<ul style="list-style-type: none"> VCC3_3: Six 0.1 μF capacitors. Less than 100 mils from package. Place near balls: A4, A1, H1, T1, AC10, and AC18. 		
2	<ul style="list-style-type: none"> VccSus3_3: Two 0.1 μF capacitors. Less than 100 mils from package. Place near balls: A22 and AC5. 		
3	<ul style="list-style-type: none"> V_CPU_IO: One 0.1 μF capacitor. Less than 100 mils from package. Place capacitor near ball AA23. 		
4	<ul style="list-style-type: none"> VCC1_5: Two 0.1 μF capacitors. Less than 100 mils from package. Place near balls: K23 and C23. 		
5	<ul style="list-style-type: none"> VccSus1_5: Two 0.1 μF capacitors. Less than 100 mils from package. Place near balls: A16 and AC1. 		
6	<ul style="list-style-type: none"> V5REF: One 0.1 μF capacitor. Less than 100 mils from package. Place capacitor near balls: E7. V5REF is the reference voltage for 5 V tolerant inputs in the Intel® ICH4. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. 		
7	<ul style="list-style-type: none"> V5REF_Sus: One 0.1 μF capacitor. Less than 100 mils from package. Place capacitor near ball: A16. V5REF_Sus only affects 5 V-tolerance for USB OC[5:0]# pins and can be connected to VccSus3_3 if 5 V tolerance on these signal is not required. 		
8	<ul style="list-style-type: none"> VccRTC: One 0.1 μF capacitor. Place near ball: AB5. 		
9	<ul style="list-style-type: none"> VCCHI: Two 0.1 μF capacitor. Less than 100 mils from package. Place near balls: T23 and N23. 		
10	<ul style="list-style-type: none"> VCCPLL: One 0.1 μF and one 0.01 μF capacitor. Within 100 mils of package. Place near ball: C22. 		

15.3 Hub Interface Layout Checklist

Table 15-4. Hub Interface Layout Checklist

No.	Recommendations	Comments	✓
General Recommendations			
1	<ul style="list-style-type: none"> It is recommended that all signals be referenced to VSS. 		
2	<ul style="list-style-type: none"> Board impedance must be $60 \Omega \pm 10\%$. 		
3	Traces must be routed as follows (see below for breakout routing requirements): <ul style="list-style-type: none"> Data to Data: 7/13 mils. Strobe to Strobe: 7/13 mils. Strobe to Data: 7/18 mils. Other signals to Data: 7/13 mils. 		
4	<ul style="list-style-type: none"> Max trace length is 8 inches. 		
Data Signals			
1	<ul style="list-style-type: none"> Can be routed to 7 on 5 for breakout, but must be separated to 5 on 15 within 300 mils of the package. 		
2	<ul style="list-style-type: none"> No explicit matching requirements between individual data signals. 		
Strobe Signals			
1	<ul style="list-style-type: none"> Strobe pair should have a minimum of 15 mils spacing from any adjacent signals. 		
2	<ul style="list-style-type: none"> Each strobe signal must be the same length. 		
3	<ul style="list-style-type: none"> Strobe trace lengths should be 0 – 400 mils shorter than the longest data trace length. 		

15.3.1 Hub Interface Decoupling, Compensation, and VREF

Table 15-5. Hub Interface Decoupling, Compensation, and VREF Checklist

No.	Recommendations	Comments	✓
VCC1_8 Decoupling			
1	• Decouple the Intel® ICH4 with two 0.1 μ F capacitors within 150 mils from the package.		
2	• Decouple the MCH with one 0.1 μ F capacitor within 150 mils of the package and one 10 μ F capacitor nearby.		
3	• Capacitors should be adjacent to hub interface rows.		
HLRCOMP			
1	• Place resistor using a 10 mils wide and 0.5 inch max trace length.		
2	• 7 mil group spacing.		
3	• Minimize the distance between HLRCOMP resistor and MCH.		
HI_REF			
1	• Should be placed no more than 4 inches of away from MCH or ICH4.		
2	• Bypass to ground with a 0.1 μ F capacitor located within 0.25 inches of each component's HIREF pin.		
3	• Place one 0.1 μ F capacitor at the divider.		

15.4 System Memory Layout Checklist

15.4.1 Unbuffered DDR (2 DIMM) Checklist

Table 15-6. Unbuffered DDR (2 DIMM) Checklist

Checklist Items	Recommendations	Comments	✓
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	Route on a ground-referenced layer (stripline for Channel A, microstrip for Channel B). MCH to first DIMM should be 1.5"–5.0", $Z_o = 50\ \Omega$, 7/15. First DIMM to second DIMM should be 1.1"–1.2", 60 Ω , 5/15. Second DIMM to termination should be 0.1"–1.5", 60 Ω , 5/15. DQ/CB lengths should be within 25 mils of associated DQS. Make sure to match the strobe lengths to the clocks as described in Section 6.2.3 .	ChA	
		ChB	
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	Route on a ground-referenced microstrip layer, $Z_o = 60\ \Omega$, 5/12. MCH to first DIMM should be 1.5"–6.5". First DIMM to second DIMM should be 1.1"–1.2". Second DIMM to termination should be 0.1"–1.5". Make sure to match the signal lengths to the clocks as described in Section 6.2.4.1 .	ChA	
		ChB	
CS_x[3:0]# CKE_x[3:0]	Route on a ground-referenced microstrip layer, $Z_o = 60\ \Omega$, 5/15. MCH to DIMM should be 1.5"–5.5", DIMM to termination should be 1.0"–2.5". Make sure to match the signal lengths to the clocks as described in Section 6.2.2.1 .	ChA	
		ChB	
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	Route differentially on a ground-referenced microstrip layer. MCH to DIMM should be 3.5"–9.0", diff. $Z_o = 84\ \Omega$, 6/7. Keep clock pairs 20 mils from any other signals. Make sure to adhere to length matching rules for above signals.	ChA	
		ChB	
VREF	Route a 12 mil wide trace to the resistor divider and to each DIMM in the channel. Keep all other signals at least 20 mils away.	ChA	
		ChB	
MCH Signals Only			
RCVENOUT_x#	Connect to resistor divider with a 7 mil wide trace. Keep the trace length to a minimum.	ChA	
		ChB	
DRCOMPVREF_H DRCOMPVREF_V	Connect to resistor divider with a 20 mil wide trace. Keep the trace length to a minimum.		
DRCOMP_H DRCOMP_V	Connect to pull-down resistor with a 7 mil wide trace. Keep the trace length to a minimum.		
DDR_STRAP	Connect to 2.5 V with a 7 mil wide trace. Keep the trace length to a minimum.		
ODTCOMP	Connect to pull-down resistor with a 7 mil wide trace. Keep the trace length to a minimum.		

15.5 AGP 8X Layout Checklist

Table 15-7. AGP 8X Layout Checklist (Sheet 1 of 3)

No.	Recommendations	Comments	✓
Power Plane Decoupling			
1	• Use high-frequency decoupling capacitors in the range of (0.001 μ F – 1 μ F).		
2	• Use bulk decoupling capacitors in the range of (0.001 μ F – 1 μ F).		
3	• Capacitors should be as close to the power pins as possible. If possible, capacitors should be mounted on the backside of the graphics card under the controller package. Bulk decoupling can be mounted near the chipset interface and near the connector for power delivery and signaling reasons.		
AC Signal Decoupling Requirements			
1	• Place 3 0.01 μ F or larger, low ESL capacitors as close as possible to a VCC3_3 pair of pins on the connector.		
2	• Place 6 0.01 μ F or larger, low ESL capacitors as close as possible to a VDDQ pair of pins on the connector.		
3	• Place 1 0.01 μ F or larger, low ESL capacitor as close as possible to the +5 V connector pin.		
4	• Place 1 0.01 μ F or larger, low ESL capacitor as close as possible to the +12 V connector pin.		
5	• Place 1 0.01 μ F or larger, low ESL capacitor as close as possible to the 3.3 Vaux connector pin.		
6	• All power and ground pins must be connected to the motherboard to guarantee power delivery and proper AC signal return paths.		
7	• All ground pins on the add-in cards must be connected for proper grounding and AC return paths. All VDDQ pins must be connected on the add-in card to the local VDDQ power plane. All used power pins must be bypassed to ground close to the connector with a 0.01 μ F or larger, low ESL/ESR capacitor to provide good AC coupling to the adjacent signaling pins.		

Table 15-7. AGP 8X Layout Checklist (Sheet 2 of 3)

No.	Recommendations	Comments	✓
Motherboard Layout Requirements			
1	<ul style="list-style-type: none"> AGP strobe signals must be grouped with associated data signals. It is also recommended that the strobe be centered within its associated group to minimize the signal to strobe skew. 		
2	<ul style="list-style-type: none"> AD_STB0 (AGP 2.0) / AD_STBFO (AGP 3.0) and AD_STB0# (AGP 2.0) / AD_STBS0 (AGP 3.0) should be grouped with AD[15:0] and C/BE[1:0]#. 		
3	<ul style="list-style-type: none"> AD_STB1 (AGP 2.0) / AD_STBF1 (AGP 3.0) and AD_STB1# (AGP 2.0) / AD_STBS1 (AGP 3.0) should be grouped with AD[31:16], C/BE[3:2]#, DBI_HI, DBI_LO (AGP 3.0). 		
4	<ul style="list-style-type: none"> SB_STB and SB_STB# should be grouped with SBA[7:0] (AGP 2.0). or <ul style="list-style-type: none"> SB_STBF and SB_STBS should be grouped with SBA[7:0]#. 		
5	<ul style="list-style-type: none"> Traces should as short and direct as possible. Avoid changing the power plane reference during routing. 		
6	<ul style="list-style-type: none"> PCB should be fabricated using FR-4 with an overall board thickness of 62 mils \pm 10%. The outer layers should use ½ copper and the inner layers should use 1 oz. copper. 		
7	<ul style="list-style-type: none"> AGP signals must be carefully routed on the motherboard and graphics card to meet the timing and signal quality requirements of the specification. 		
Trace Length Mismatch Requirements			
1	<ul style="list-style-type: none"> Avoid signal mismatch by routing all lines within a group using the same type (either stripline or microstrip). 		
2	<ul style="list-style-type: none"> For add-in cards, the data lines should be kept within \pm 0.025 inches from their respective strobe. 		
3	<ul style="list-style-type: none"> For motherboards, the data lines should be kept within \pm 0.025 inches from their respective strobe. 		
Strobe Trace Routing Considerations			
1	<ul style="list-style-type: none"> The strobe signals should be routed together, but separated by at least five times the maximum dielectric thickness to each other and to any other signal routed adjacent to the strobe. 		
Board Constraints			
1	<ul style="list-style-type: none"> Impedance of required microstrip traces is specified at $60 \Omega \pm 10\%$ and the impedance for stripline traces is specified at $56 \Omega \pm 10\%$ for add-in cards and motherboards. 		
2	<ul style="list-style-type: none"> Reduce crosstalk by decreasing the distance of a trace to the nearest reference plane (dielectric thickness/height). Or increase the distance to adjacent traces. 		
3	<ul style="list-style-type: none"> The 8X mode source synchronous signals and the 66 MHz clock signal should not cross any split planes. Ensure signal quality is not compromised. 		
4	<ul style="list-style-type: none"> All 8X mode source synchronous signals should be routed on a layer reference to a ground plane. 		
5	<ul style="list-style-type: none"> Dummy vias should be used to match the total via count for each group. 		

Table 15-7. AGP 8X Layout Checklist (Sheet 3 of 3)

No.	Recommendations	Comments	✓
Control Signal and Clock Recommendations			
1	<ul style="list-style-type: none"> There are no external pull-up or pull-down resistors for control signals on the AGP 8X mode board design since resistors are integrated inside the device buffers. 		
Ground Plane References			
1	<ul style="list-style-type: none"> Each source synchronous signal group must be routed on the same layer referenced to ground with the same layer transitions. 		
VDDQ Plane			
1	<ul style="list-style-type: none"> The plane from the voltage regulator source to the AGP connector VDDQ pins should be wide enough to minimize the inductance path. 		
2	<ul style="list-style-type: none"> Buffer I/O rail on the add-in card should connect to the VDDQ plane directly. 		
Connector Impedance Matching			
1	<ul style="list-style-type: none"> The motherboard designer can put short trace stubs near each connector pin to increase the equivalent capacitance which can help reduce the AGP connector impedance. 		
Trace Bends and Serpentes			
1	<ul style="list-style-type: none"> Void 90 degrees bends, instead use two 45 degree bends. Trace bends and serpentes generate coupling causing the line to be shorter electrically. 		

15.6 CK 408 Layout Checklist

Table 15-8. CK 408 Layout Checklist (Sheet 1 of 3)

No.	Recommendations	Comments	✓
Host Clock: CPU#/CPU			
1	• 7 mils wide.		
2	• Differential pair spacing should be based on a distance from HCLKINN to HCLKINP.		
3	• Spacing to other traces should 4 times to 5 times greater than distance from HCLKINN to HCLKINP.		
4	• Processor routing length- Clock driver to R_S should be 0.5 inch max.		
5	• Processor routing length- R_S to R_S-R_T should be 0 inch to 0.2 inch.		
6	• Processor routing length- R_S-R_T node to R_T should be 0 inch to 0.2 inch.		
7	• Processor routing length- R_S-R_T node to load should be 2 inches to 9 inches.		
8	• MCH routing length- Clock driver to R_S should be 0.5 inch max.		
9	• MCH routing length- R_S to R_S-R_T should be 0.5 inch max.		
10	• MCH routing length- R_S-R_T node to R_T should be 0.0 inch to 0.2 inch max.		
11	• MCH routing length- R_S-R_T node to load should be 2.0 inches to 9.0 inches max.		
12	• Clock driver to processor and clock driver to chipset length matching should be 600 mils.		
13	• 10 mil length matching between HCLKINN to HCLKINP.		
14	• Do not split up the two halves of a differential clock pair between layers.		
15	• Route all agents on the same physical routing layer referenced to ground of the differential clock.		
16	• Make sure that the skew induced by the vias is compensated in the traces to other agents.		
17	• Do not place vias between adjacent complementary clock traces.		
18	• Maintain uniform spacing between the two halves of differential clocks.		
19	• Route clocks on physical layers adjacent to the VSS reference plane only.		

Table 15-8. CK 408 Layout Checklist (Sheet 2 of 3)

No.	Recommendations	Comments	√
66 MHz Clock Group			
1	• Point-to-point Topology.		
2	• 5 mils wide and 20 mil spacing.		
3	• 20 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 4.0 inches and 8.5 inches.		
6	• The total trace lengths must be matched to ± 100 mils of each other.		
7	• Follow these guidelines when routing to an AGP device down on the motherboard.		
AGP Clock (when routing to an AGP connector)			
1	• Point-to-point Topology.		
2	• 5 mils wide and 20 mil spacing.		
3	• 20 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length must be 4.0 inches less than the CLK66 total trace lengths ± 100 mils.		
33 MHz Clock Group			
1	• Point-to-point Topology.		
2	• 5 mils wide and 15 mil spacing.		
3	• 15 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total mismatch between any two 33 MHz clocks must be less than 7.5 inches. If routing to a PCI connector, 2.6 inches of routing on the PCI card must be included in the 7.5 inches total mismatch.		
6	• The 33 MHz clock to the Intel® ICH4 must be matched to ± 100 mils of the 66 MHz clock to the ICH4.		
14 MHz Clock Group			
1	• Balanced T Topology.		
2	• 5 mils wide and 10 mil spacing.		
3	• 10 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length from the Clock driver to SIO and Clock driver must be matched to 0.5 inch.		
6	• Signal must T within 12 inches of the series termination. • Max trace length of stubs is 6 inches.		
7	• Total trace length matched to ± 0.5 inch of each other.		

Table 15-8. CK 408 Layout Checklist (Sheet 3 of 3)

No.	Recommendations	Comments	✓
USB Clock			
1	• Point-to-point Topology.		
2	• 5 mils wide.		
3	• 15 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 3.0 inches and 12 inches.		

15.6.1 CK 408 Decoupling Checklist

Table 15-9. CK 408 Decoupling Checklist

No.	Layout Recommendations	Comments	✓
VDDA/VDD Decoupling			
1	• Place one 10 μ F capacitor close to the VDD generation circuitry.		
2	• Place six 0.1 μ F capacitors close to the VDD pins on the clock driver.		
3	• Place three 0.01 μ F capacitors close to the VDDA pins on the clock driver.		
4	• Place one 10 μ F bulk decoupling capacitor close to the VDDA generation circuitry.		
5	• Host clock pairs must be differentially routed on the same physical routing layer.		
6	• Differential clocks must not have more than two via transitions.		
7	• Ground referencing is strongly recommended for all platform clocks.		
8	• Motherboard layer transitions and power plane splits must be kept to a minimum.		

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Schematics

A

This appendix contains a set of schematics for the Intel® Pentium® 4 processor / Intel® E7205 chipset platform Customer Board (CRB).

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CR-1 8		7		6		5		4		3		2		1	
D	PAGE	COMPONENT / FUNCTION		PAGE	COMPONENT / FUNCTION		<div>INTEL(R) PENTIUM(R) 4 PROCESSOR- INTEL(R) E7205 CHIPSET CUSTOMER REFERENCE SCHEMATICS</div> <div>THESE SCHEMATICS ARE PROVIDED AS IS WITH NO WARRANTIES WHATSOEVER INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF PROPOSAL, SPECIFICATION OR SAMPLES.</div> <div>INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT, EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS. INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS. INTEL MAY MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME, WITHOUT NOTICE.</div> <div>THE INTEL(R) E7505 CHIPSET MAY CONTAIN DESIGN DEFECTS OR ERRORS KNOWN AS ERRATA WHICH MAY CAUSE THE PRODUCT TO DEVIATE FROM PUBLISHED SPECIFICATIONS. CURRENT CHARACTERIZED ERRATA ARE AVAILABLE ON REQUEST.</div> <div>INTEL MAY MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE.</div> <div>COPYRIGHT (C) INTEL CORPORATION 2002.</div> <div>*THIRD-PARTY BRANDS AND NAMES ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS.</div>								
	1	INDEX		50	AUDIO CONNECTORS										
	2	BLOCK DIAGRAM		51	AUDIO MIC IN										
	3	RESET MAP		52	AUDIO										
	4	CLOCK DISTRIBUTION		53	AUDIO FRONT PANEL										
	5	GPIO / IRQ / IDSEL		54	AUDIO VREG										
	6	CPU SOCKET		55	SP DIF / CUSTOM FEATURE										
	7	CPU TERMINATION		56	TRUSTED PLATFORM MODULE										
	8	CPU PLL FILTERS		57	1394 USB FRONT PANEL HDR										
	9	MCH		58	1394 CONTROLLER										
C	10	MCH		59	SATA VREG										
	11	MCH		60	SATA CONTROLLER										
	12	MCH		61	PORT ANGELES(PART 1)/SIO										
	13	MCH TERMINATION		62	FLOPPY CONNECTOR										
	14	CLOCK		63	PS2 KEYBOARD / MOUSE										
	15	AGP PRO CONNNECTOR		64	PARALLEL PORT										
	16	BLANK		65	COM1 PORT										
	17	CH A DDR DIMMS		66	FWH										
	18	CH A DDR DATA TERM		67	PORT ANGELES(PART 2)/GLUE4										
	19	CH A DDR CONTROL TERM		68	HECETA										
B	20	CH A DIMM DECOUPLING		69	SPEAKER										
	21	BLANK		70	FRONT PANEL HEADER										
	22	CH B DDR DIMMS		71	MOUNTING HOLES										
	23	CH B DDR DATA TERM		72	FAN CONTROL										
	24	CH B DDR CONTROL TERM		73	SMBUS ISOLATION MAP										
	25	CH B DIMM DECOUPLING		74-76	SPECIAL HEADERS										
	26	ICH		77	VREG MAP										
	27	ICH		78	2.5V VREG										
	28	ICH POWER/GND		79	1.25V VREG										
	29	ICH		80	POWER SUPPLY CONN / 12V										
A	30	ICH TERMINATION		81	BATTERY & PCIV AUX										
	31	ICH LAN LINK		82	VREG BP RIGHT USB / PS2										
	32	IDE CONNECTORS		83	VREG BACKPANEL USB										
	33	USB BACK PANEL		84	3.3V STBY / 1.5V STBY										
	34	USB FP HDR / POWER		85	VREG DECOUPLING										
	35	USB BPR / FP HDR		86	1.3V VREG										
	36	PCI SLOTS		87	1.5V VREG										
	37	PCI SLOT4		88	CPU VREG										
	38	PCI SLOT3		89	CPU VREG DECOUPLING										
	39	PCISLOT2		90-93	BLANK										
	40	PCI SLOT1		94	BACKSIDE DECOUPLING										
	41	PCI TERMINATION		95	DEBUG POWER LEDS										
	42	PCI ARBITER		96	PWR BUTTON / VID STRAPS										
	43	CNR		97	TDR COUPONS										
	44	LAN CONTROLLER		98	DEBUG HEADERS										
	45	LAN POWER / GND		99	LPC DEBUG / PORT 80										
	46	LAN CONTROL / EEPROM		100	ITP										
	47	LAN / USB CONNECTOR		101	SIGNAL CROSS REFERENCE										
	48	AUDIO CODEC		106	UNIT CROSS REFERENCE										
	49	AUDIO													

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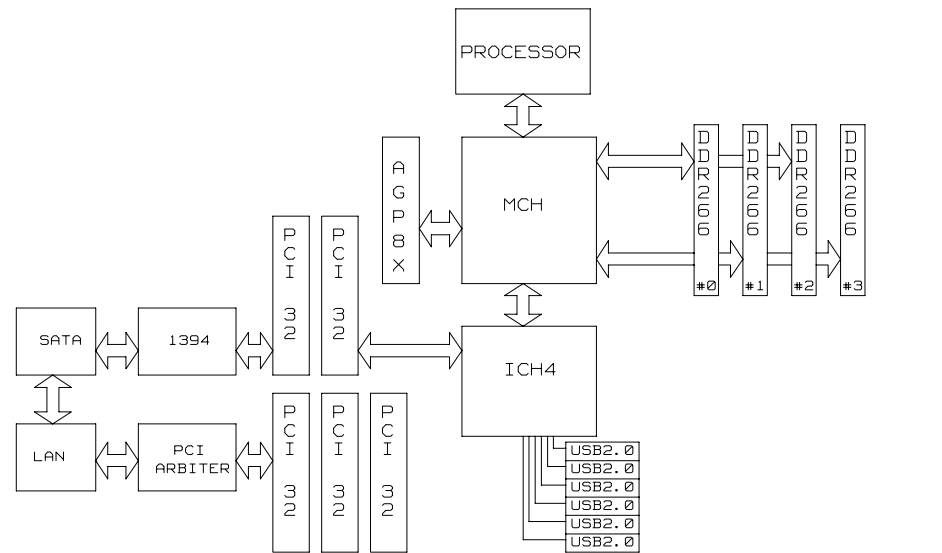
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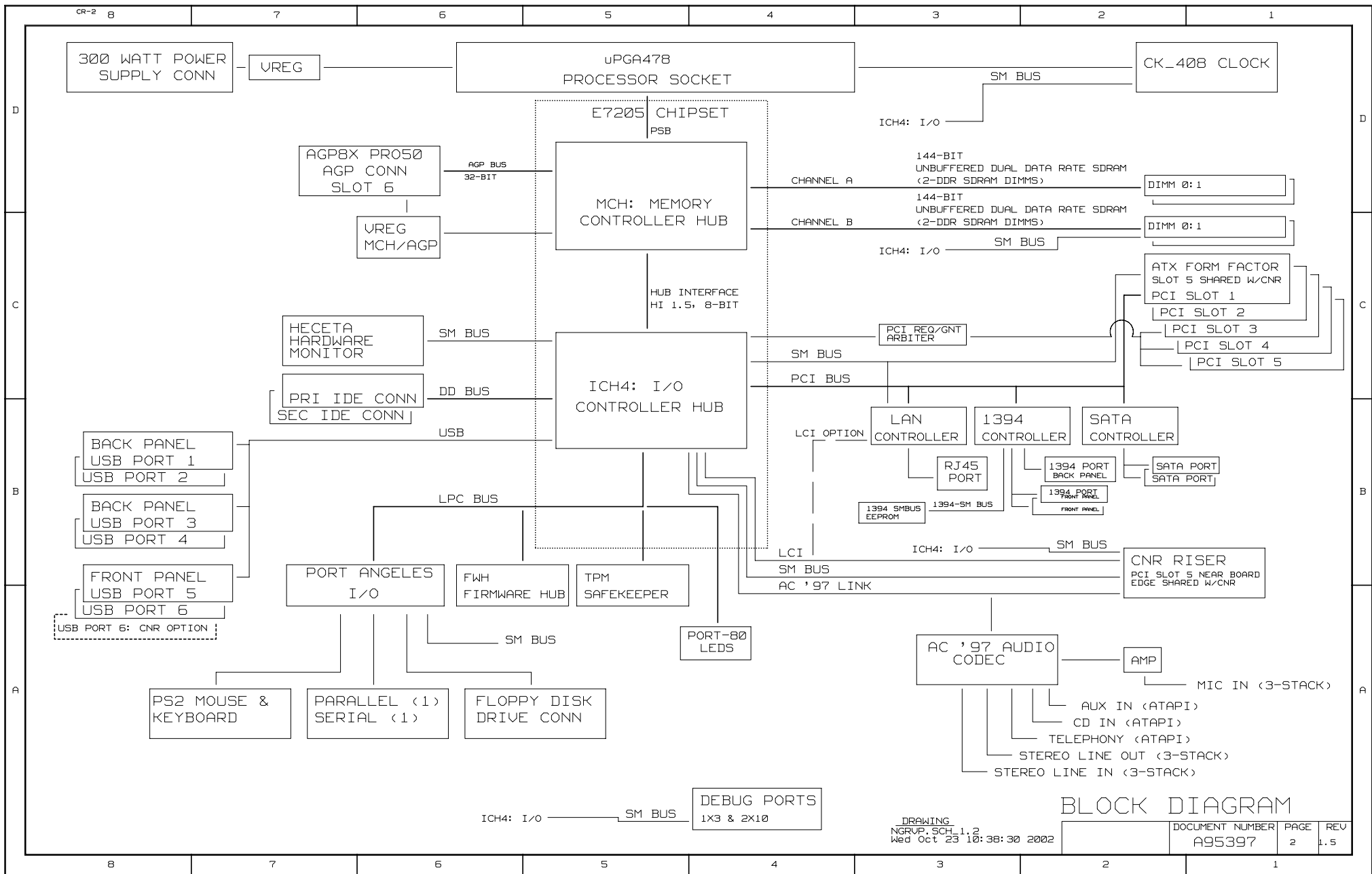
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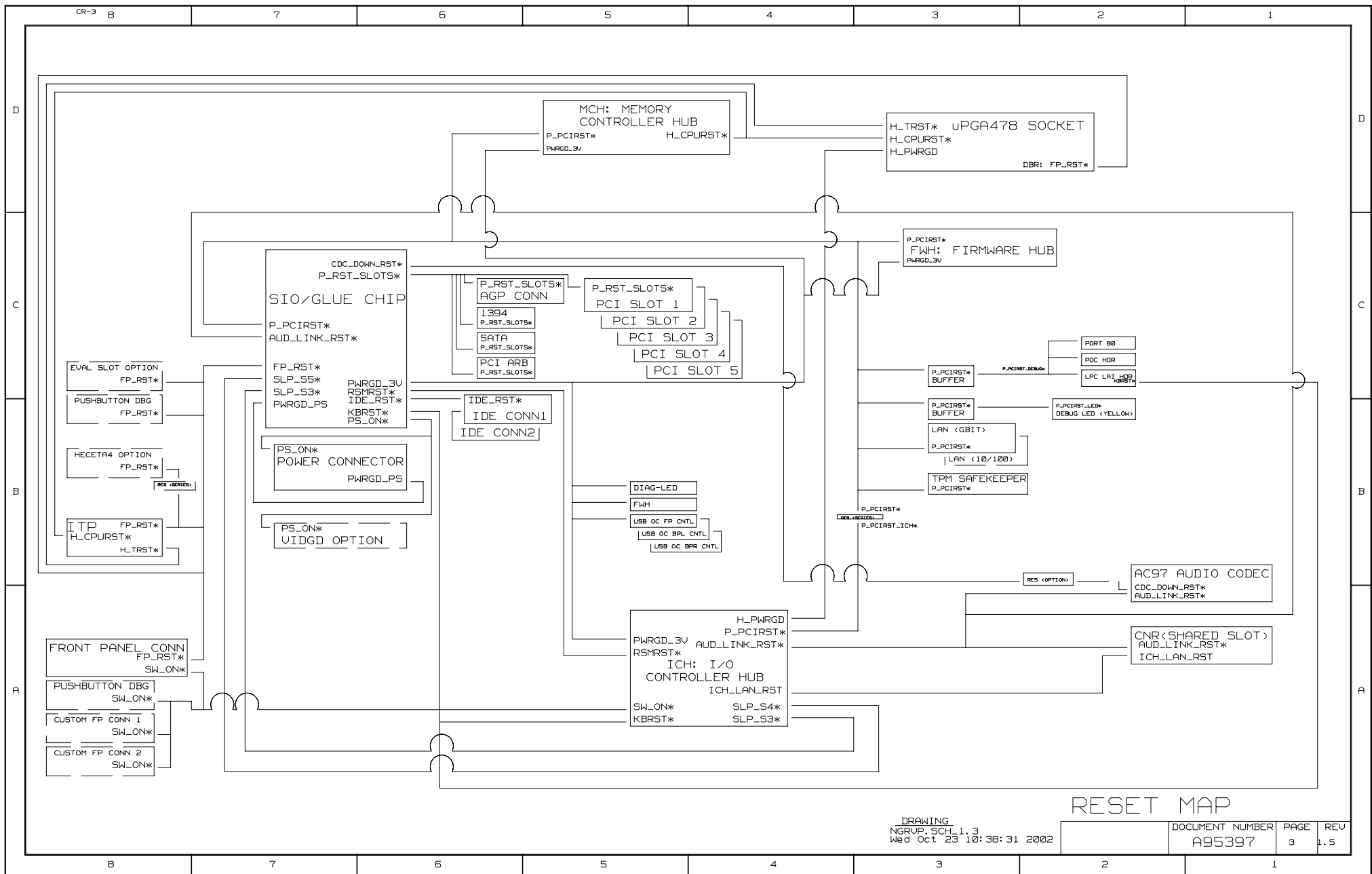
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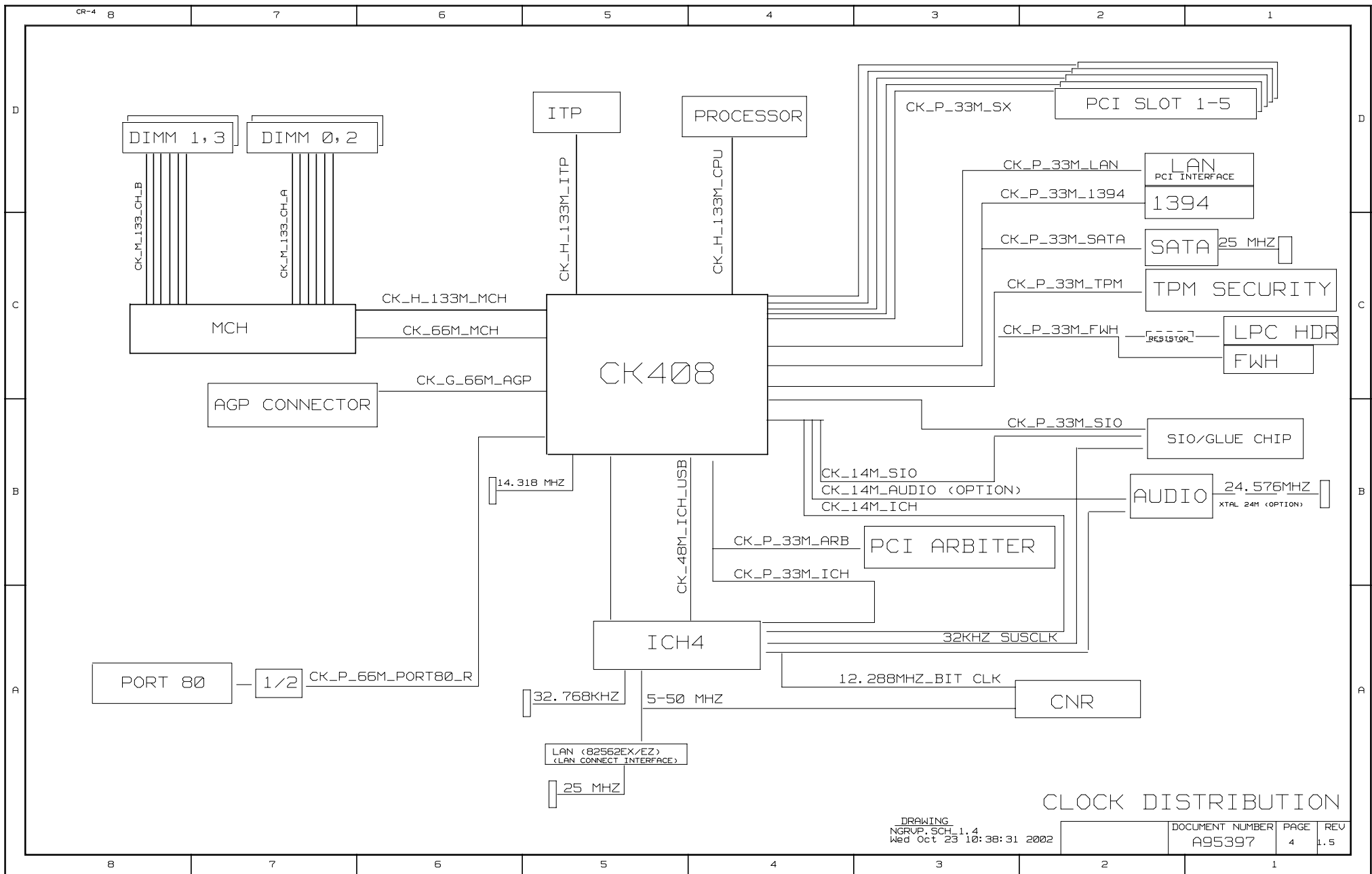


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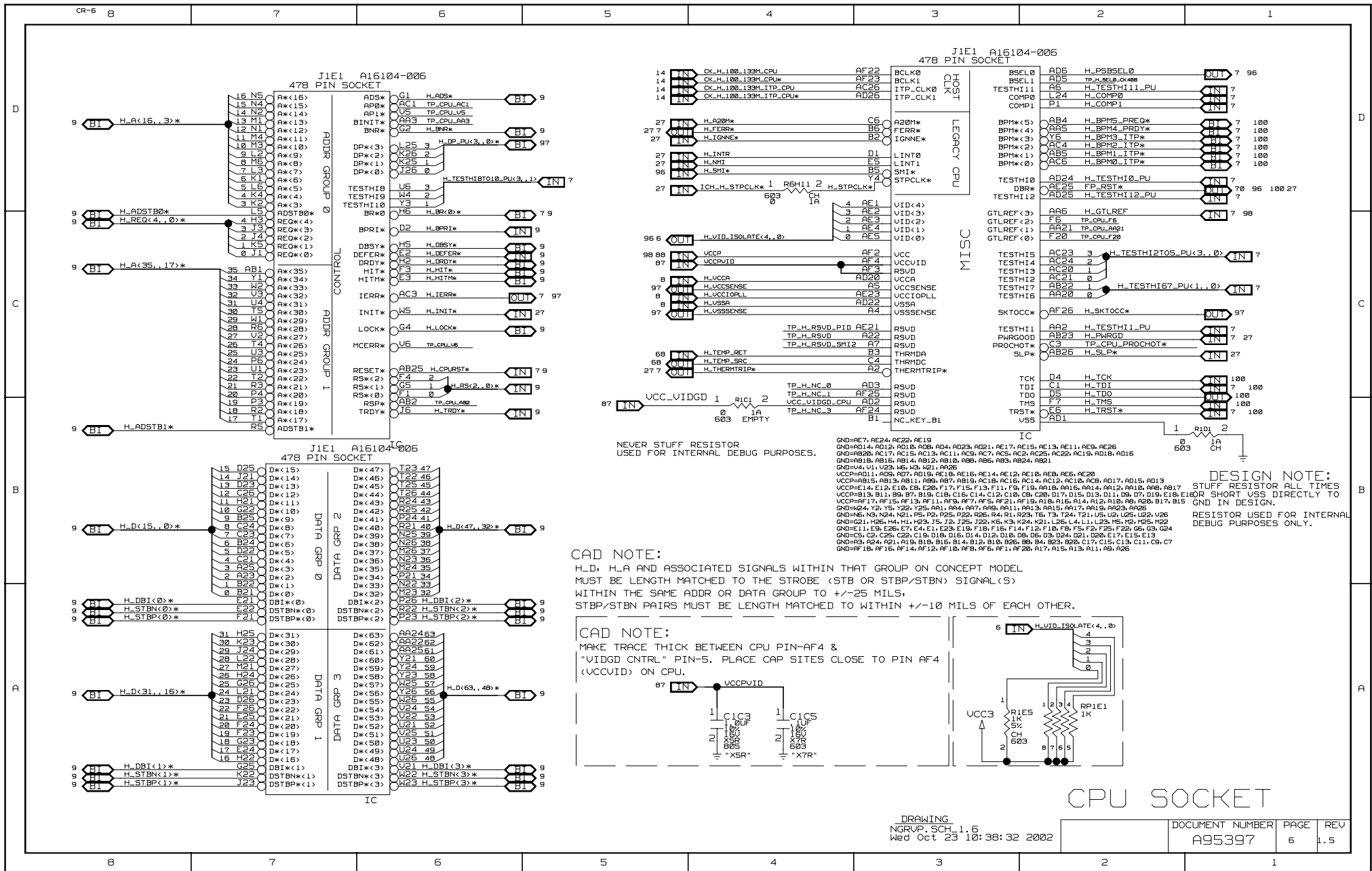
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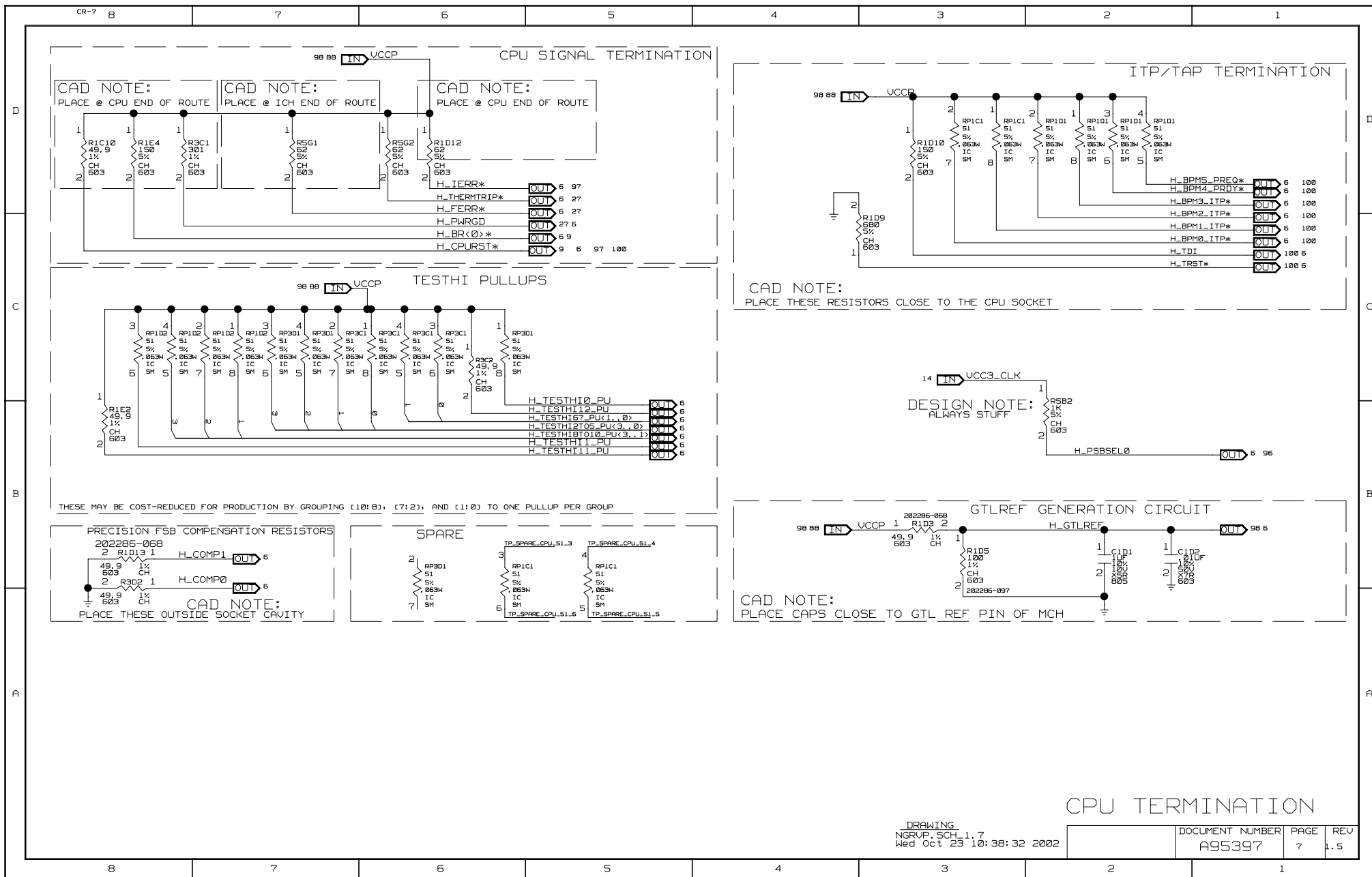






CR-5 8		7		6		5		4		3		2		1								
D	ICH	PIN NAME	POWER WELL	USAGE	AFTER RSMRST	DURING S3/S5	NOTES															
		GPI00	MAIN	P_REQA*	---	---	P/U ON PG 41, 2.7K TO VCC5															
		GPI01	MAIN	P_REQ5*	---	---	P/U ON PG 41, 2.7K TO VCC5, USED ON LAN															
		GPI02	MAIN	P_INTE*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS															
		GPI03	MAIN	P_INTF*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS, SATA															
		GPI04	MAIN	P_INTG*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS															
		GPI05	MAIN	P_INTH*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS															
		GPI06	MAIN	AGPBUSY-NOT USED	---	---	P/U ON PG 30, 10K TO VCC3 (STRAPPED TOGETHER WITH GP7)															
		GPI07	MAIN	AVAILABLE-NOT USED	---	---	P/U ON PG 30, 10K TO VCC3 (STRAPPED TOGETHER WITH GP6)															
		GPI08	RESUME	CDC_DWN_ENAB*	---	---	P/D ON PG 30, 10K TO GROUND (EMPTY 100K P/U TO 3.3V STBY)															
		GPI011	RESUME	SMB_ALERT-NOT USED	---	---	P/U ON PG 30, 10K TO 3.3VSB															
		GPI012	RESUME	LPC_SIO_SMI*	---	---	P/U ON PG 61, 10K TO 3.3V STBY, USED ON PORT ANGELES IO_SMI/GPI04															
		GPI013	RESUME	LPC_SIO_PME*	---	---	P/U ON PG 61, 10K TO 3.3V STBY, USED ON PORT ANGELES IO_PME															
		GP0016	MAIN	P_GNTA*	HIGH	OFF	EMPTY P/D ON PG 41, 10K TO GROUND															
		GP0017	MAIN	P_GNT5*	HIGH	OFF	USED ON LAN															
		GP0018	MAIN	STAPCI-NOT USED	HIGH	OFF																
		GP0019	MAIN	SLP_S1-NOT USED	HIGH	OFF																
		GP0020	MAIN	STPCPU-NOT USED	HIGH	OFF																
		GP0021	MAIN	C3_STAT-NOT USED	HIGH	OFF																
		C	ICH	GP0022	MAIN	CPU_PERF-NOT USED	HI-Z	OFF	P/U ON PG 30, 10K TO VCC3 (O/D OUTPUT)													
GP0023	MAIN			GMUXSEL-NOT USED	LOW	OFF																
GPI0024	RESUME			CLK_RUN-NOT USED	LOW	DEFINED																
GPI0025	RESUME			GPIO_GRP_BLNK- NOT USED	HIGH	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE															
GPI0027	RESUME			GPIO_YLW_BLNK- NOT USED	HIGH	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE															
GPI0028	RESUME			GPIO_LAN_DISABLE/EMAILLED	HIGH	DEFINED	P/D ON PAGE 27, 10K TO GROUND, GPIO 25, 27, 28 ARE BLINK CAPABLE															
GPI0032	MAIN			GPIO_MUTE_AUDIO-NOT USED	---	---																
GPI0033	MAIN			GPIO_AUD_EN- NOT USED	---	---																
GPI0036	MAIN			AVAILABLE-NOT USED	---	---																
GPI0037	MAIN			BOARD_SKU0	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)															
GPI0038	MAIN			BOARD_SKU1	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)															
GPI0039	MAIN			BOARD_SKU2	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)															
GPI0040	MAIN			BOARD_SKU3	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)															
GPI0041	MAIN			AGPPRO_PRESENT1	---	---	CONNECTED TO AGPPRO CONNECTOR															
GPI0042	MAIN			AGPPRO_PRESENT2	---	---	CONNECTED TO AGPPRO CONNECTOR															
GPI0043	MAIN			RSVD-BOARD_SKU4	---	---	P/D ON PAGE 30, 10K P/U TO VCC3 (EMPTY 10K TO GND)															
B	FWH			GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED	P/D ON PAGE 32, 15K TO GROUND													
				GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED	P/D ON PAGE 32, 15K TO GROUND													
				GPI2		AVAILABLE-NOT USED	INPUT	DEFINED	P/D ON PAGE 66, 10K TO GROUND (EMPTY 10K P/U TO VCC3): COM2 DETECT IF P-UP													
				GPI3		MANUFACTURING MODE	INPUT	DEFINED	P/U ON PAGE 66, 4.7K TO VCC3 (EMPTY PAD-SITE TO ALLOW ICT PROBE)													
		GPI4		NORMAL/CONFIG/RECOVERY BIOS	INPUT	DEFINED	P/D ON PAGE 66, 4.7K TO GROUND (HEADER TO ALLOW 1K P/U TO VCC3)															
		A	SIO/GLUE	GPI00		FAN1_CTRL (TRISTATE @PWRGD)	---	OUTPUT	PAGE 68-72; DESIGN FEATURE WITH EMPTY P/U, EMPTY FET FOR FAN EXP.													
				GPI01		FAN2_CTRL (TRISTATE @PWRGD)	---	OUTPUT	P/U ON PG 72, 1K TO VCC3													
				GPI02		DIAGLED-DATA- RESISTOR CFG OPTION	---	OUTPUT	PAGE 96-92; DESIGN FEATURE WITH P/U, P/D RESISTOR STRAPPING													
				GPI03		DIAGLED-STB- RESISTOR CFG OPTION	---	OUTPUT	PAGE 96-92; DESIGN FEATURE WITH P/U, P/D RESISTOR STRAPPING													
				GPI04		IO_SMI* (TRISTATE @PWRGD)	---	OUTPUT	P/U ON PG 61, 10K TO 3.3V STBY, USED ON ICH IO_SMI/GPI12													
				GPI05		AVAILABLE-NOT USED (TRISTATE@PWR)	---	OUTPUT	EMPTY P/U, P/D PAGE 61; OPTION FOR FORCING SIO ADDRESS SELECT													
				IO_PME*		IO_PME* (INACTIVE @ PWRGD)	---	OUTPUT	P/U ON PG 61, 10K TO 3.3V STBY, USED ON ICH IO_PME/GPI13													
				GPI06, 7		FAN_TACH1 & 2, (TRISTATE @PWRGD)	---	INPUT	PAGE 72; 10K PULL-UP TO 12V (THROUGH A VOLTAGE DIVIDER)													
				IRQ ROUTING TABLE																		
				ICH SIGNALS	AGP	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	ICH4 AC97, SMBUS	ICH4 LAN	ICH4 USB #1	ICH4 USB #2	ICH4 USB #3	ICH4 USB 2.0	KENAI LAVON LAN	SATA	1394		
				P_INTA*	IRQA			IRQD		IRQC				X						IRQA		
				P_INTB*	IRQB			IRQC		IRQA	N/A	X								IRQA		
				P_INTC*				IRQA	IRQB							X		IRQA				
				P_INTD*				IRQB	IRQA													
				P_INTE*		IRQD	IRQC			IRQD			X									
P_INTF*				IRQA	IRQB			IRQC									IRQA					
P_INTG*				IRQB	IRQA			IRQD														
P_INTH*				IRQC	IRQD			IRQB							X							
REQ/GNT				0	1	ARB-2	ARB-3	ARB-4	N/A		5					5	4	3				
IDSEL				16	17	18	19	20	N/A		24					21	22	23				
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NGRUP, SCH.1.5																						
Wed Oct 23 10:38:31 2002																						
DOCUMENT NUMBER																						
A95397																						
PAGE																						
5																						
REV																						
1.5																						
8		7		6		5		4		3		2		1								

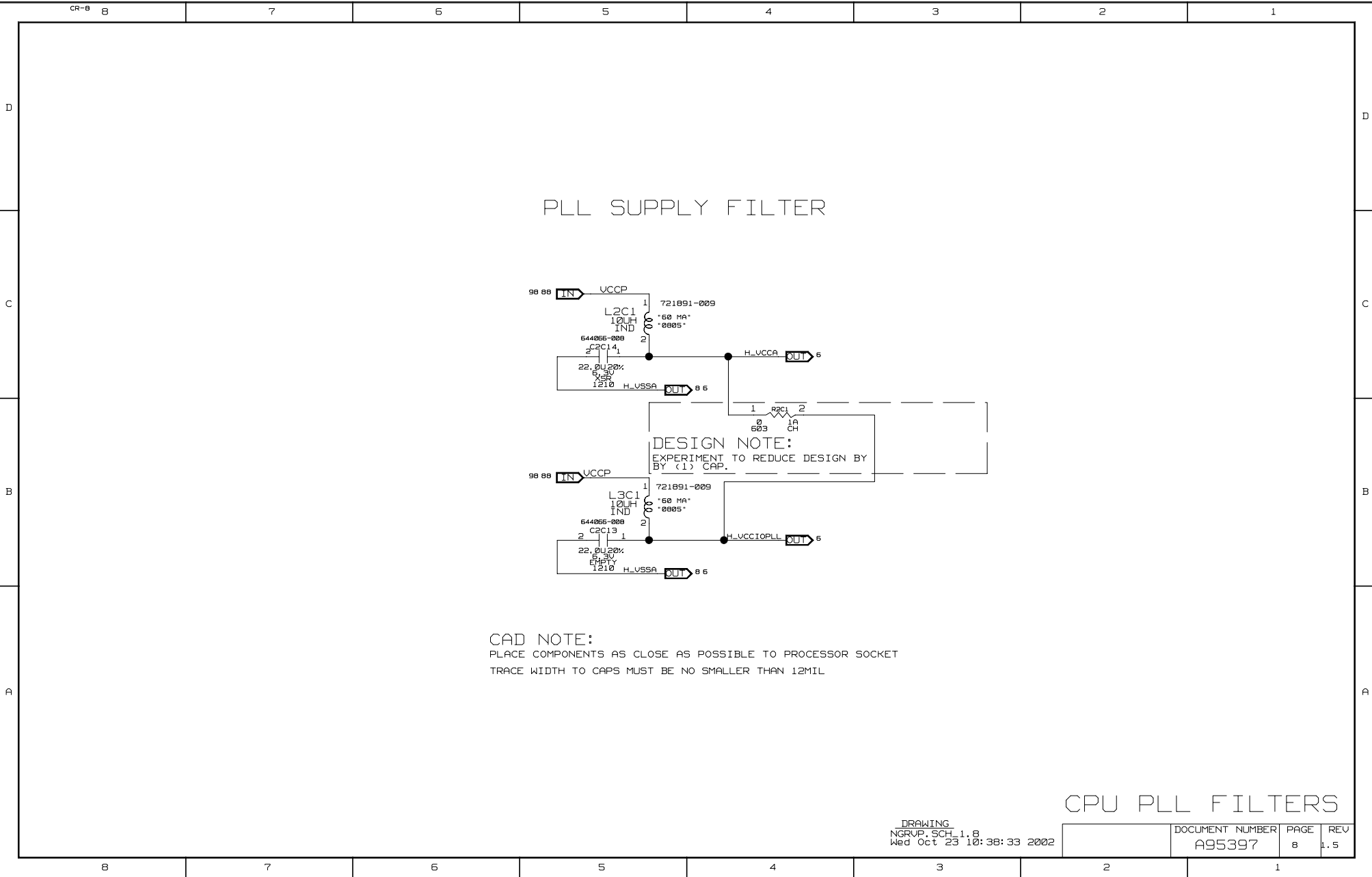


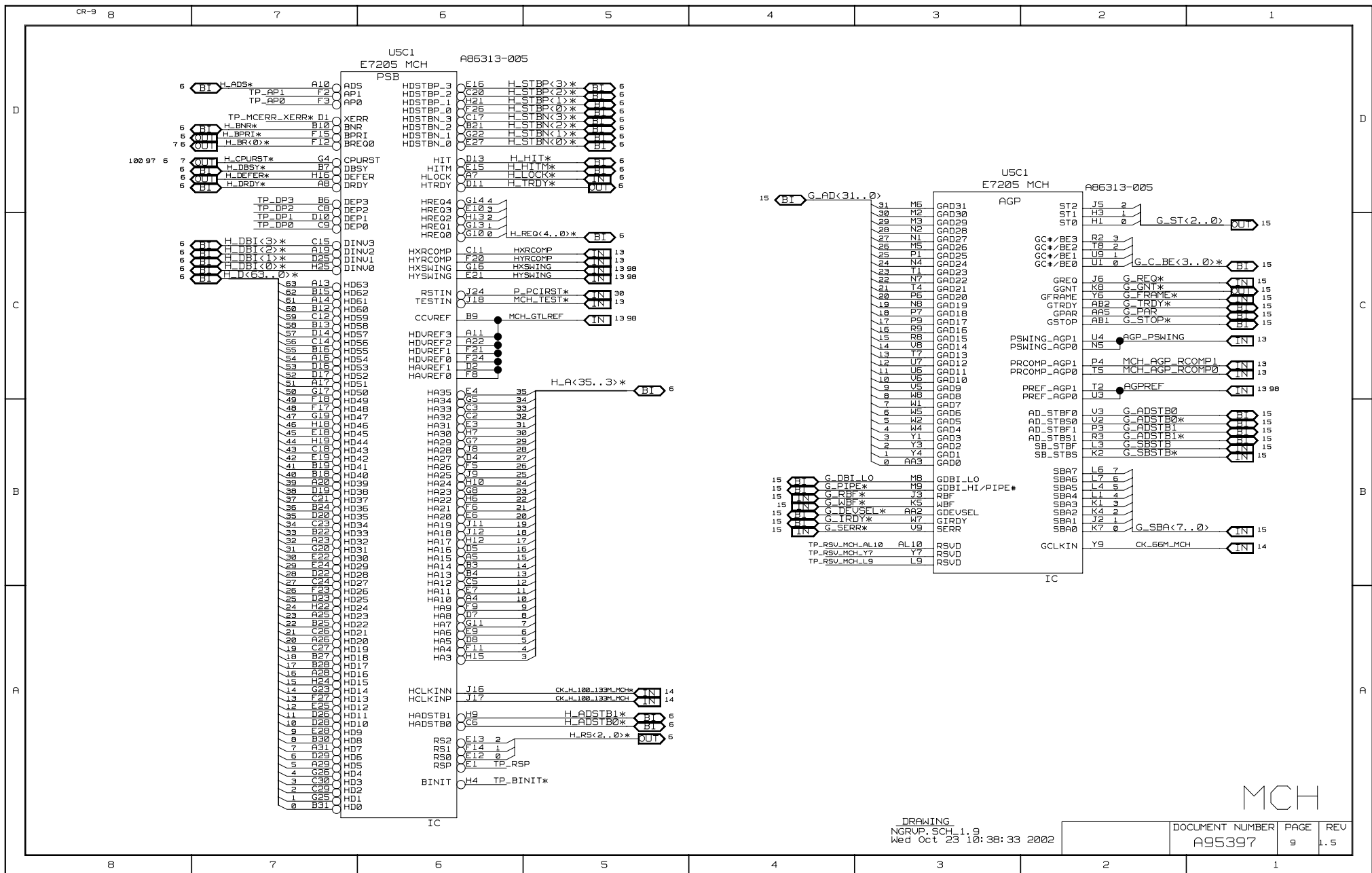


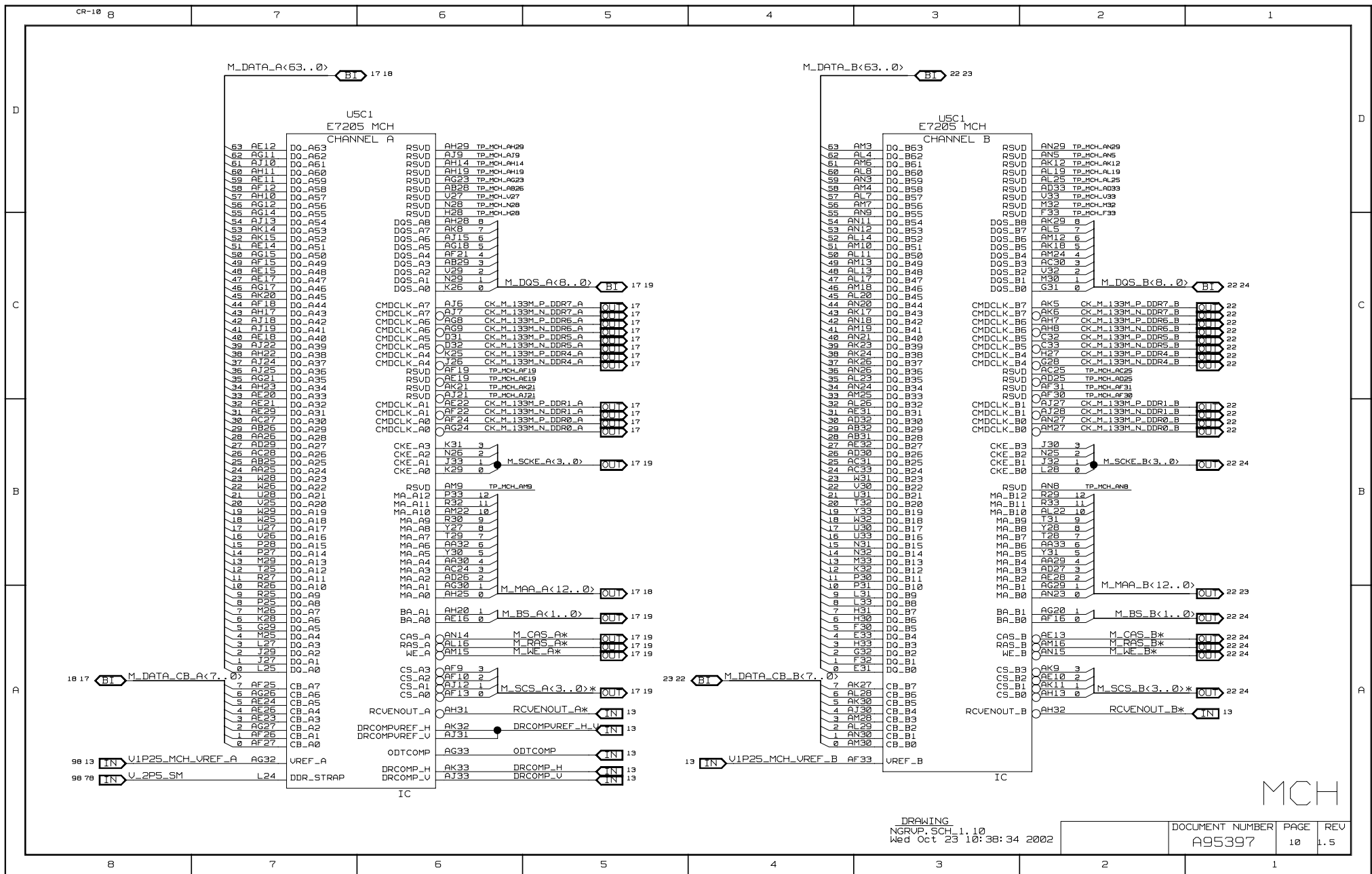
CPU TERMINATION

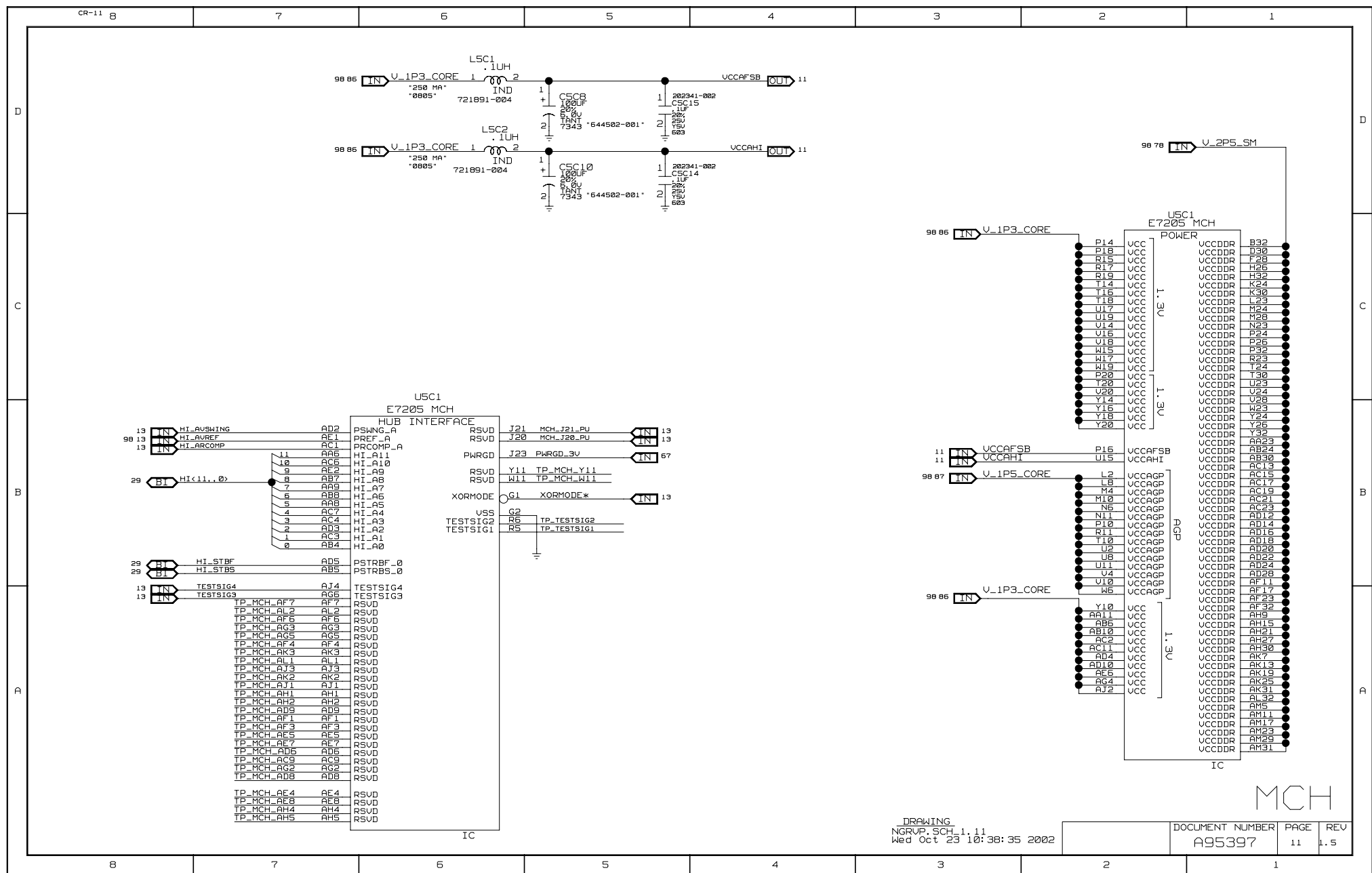
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NGRUP_SCH_1.7
Wed Oct 23 10:38:32 2002

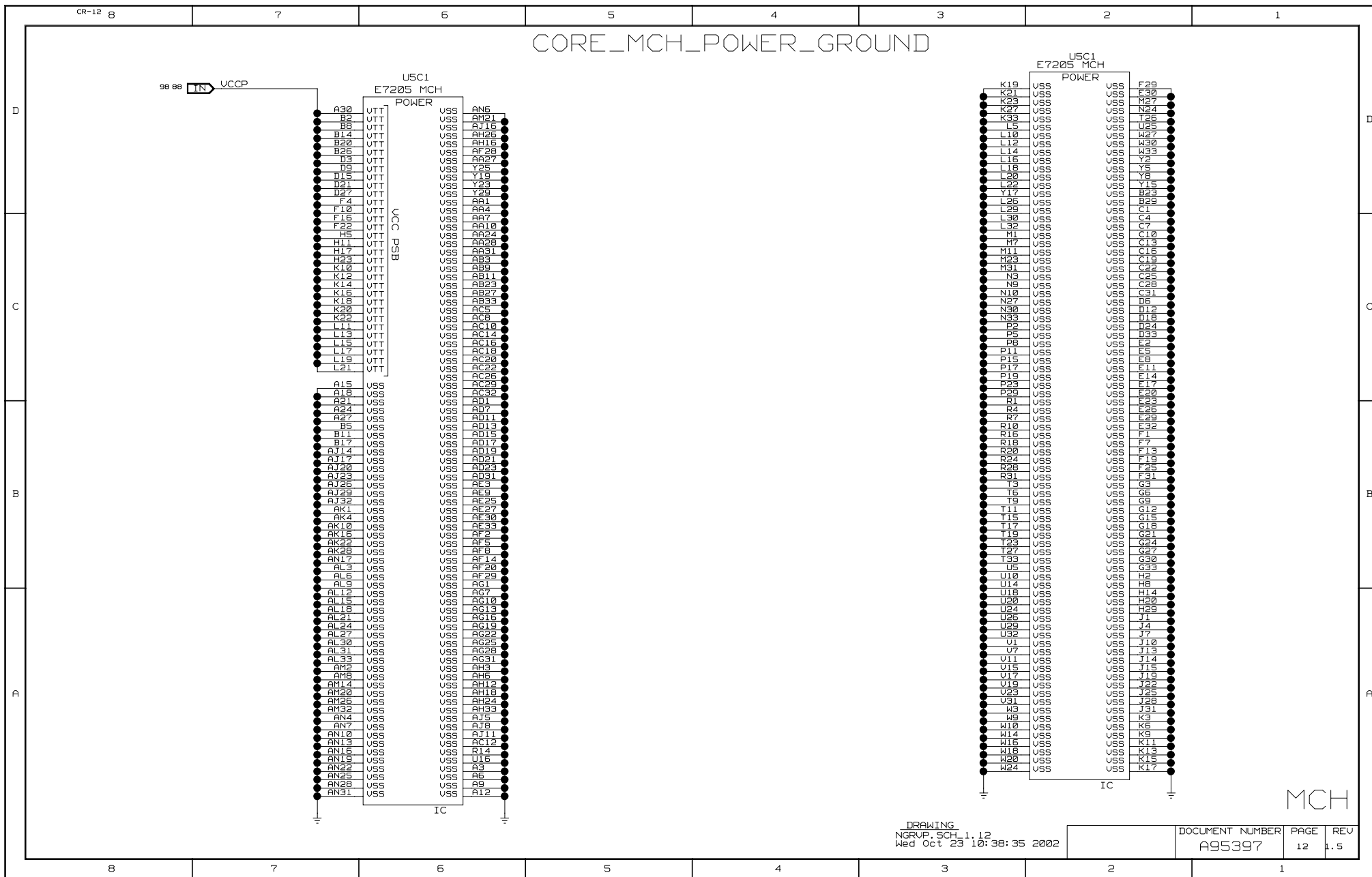
DOCUMENT NUMBER A95397	PAGE 7	REV 1.5
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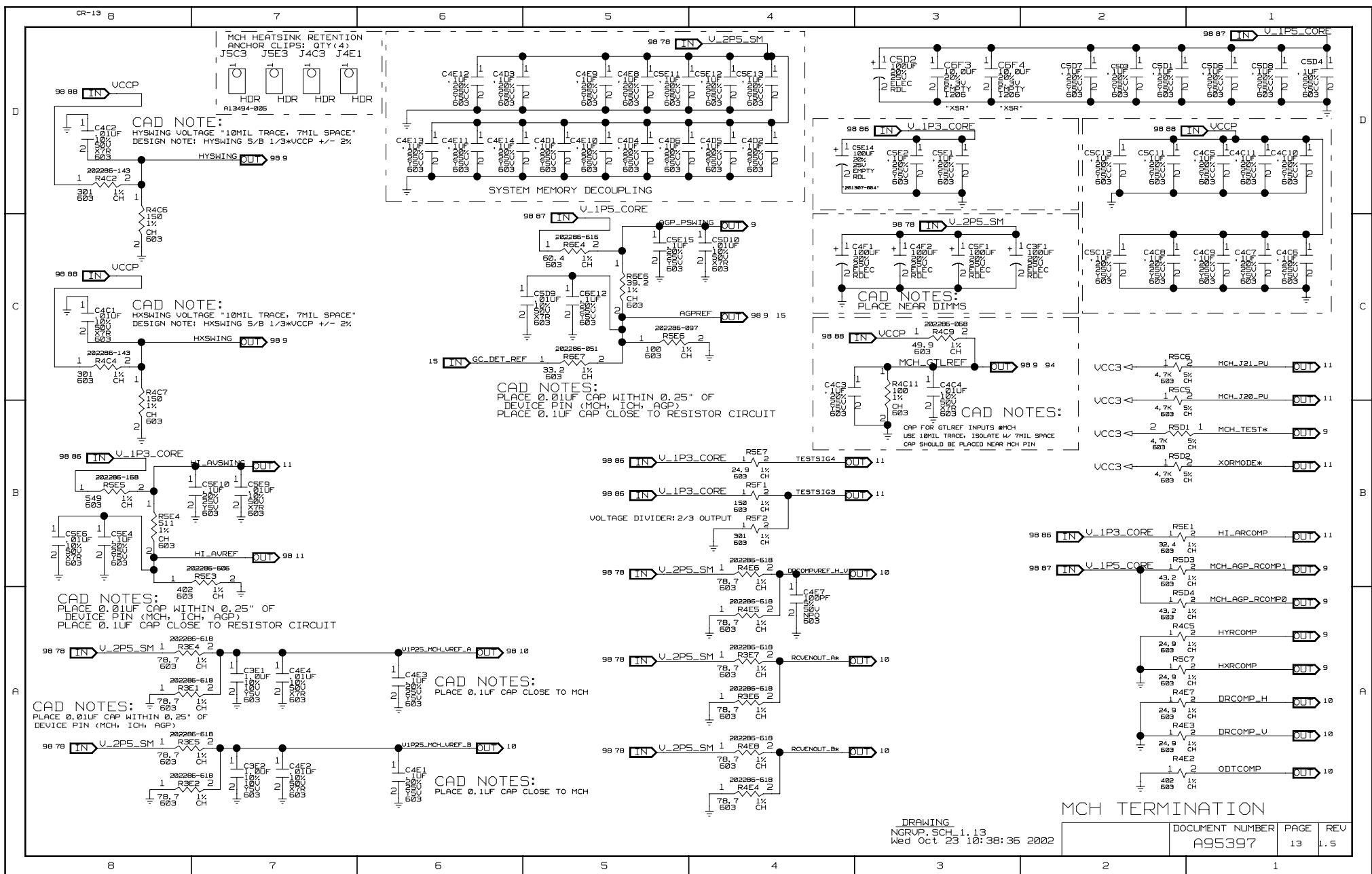


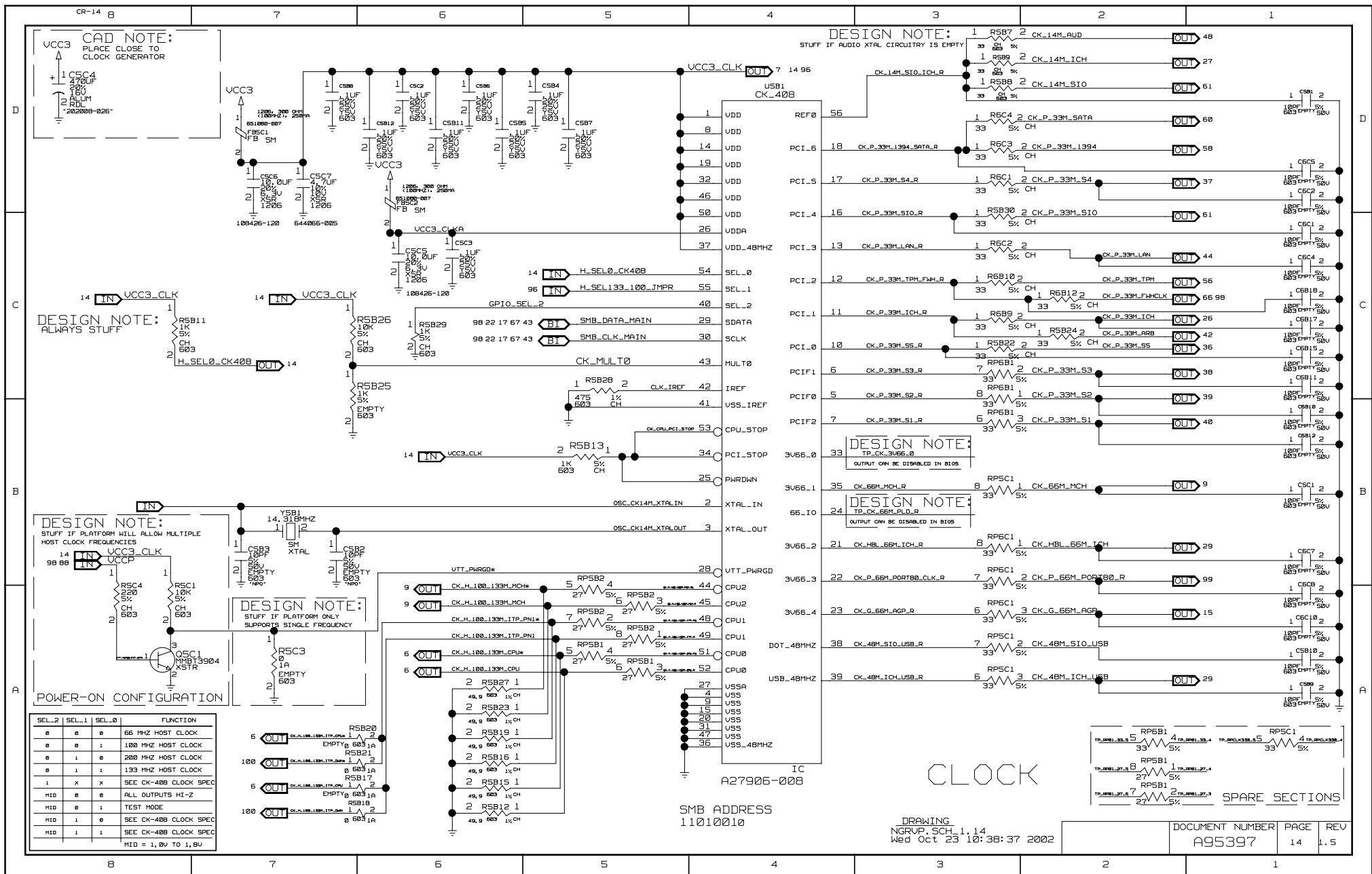


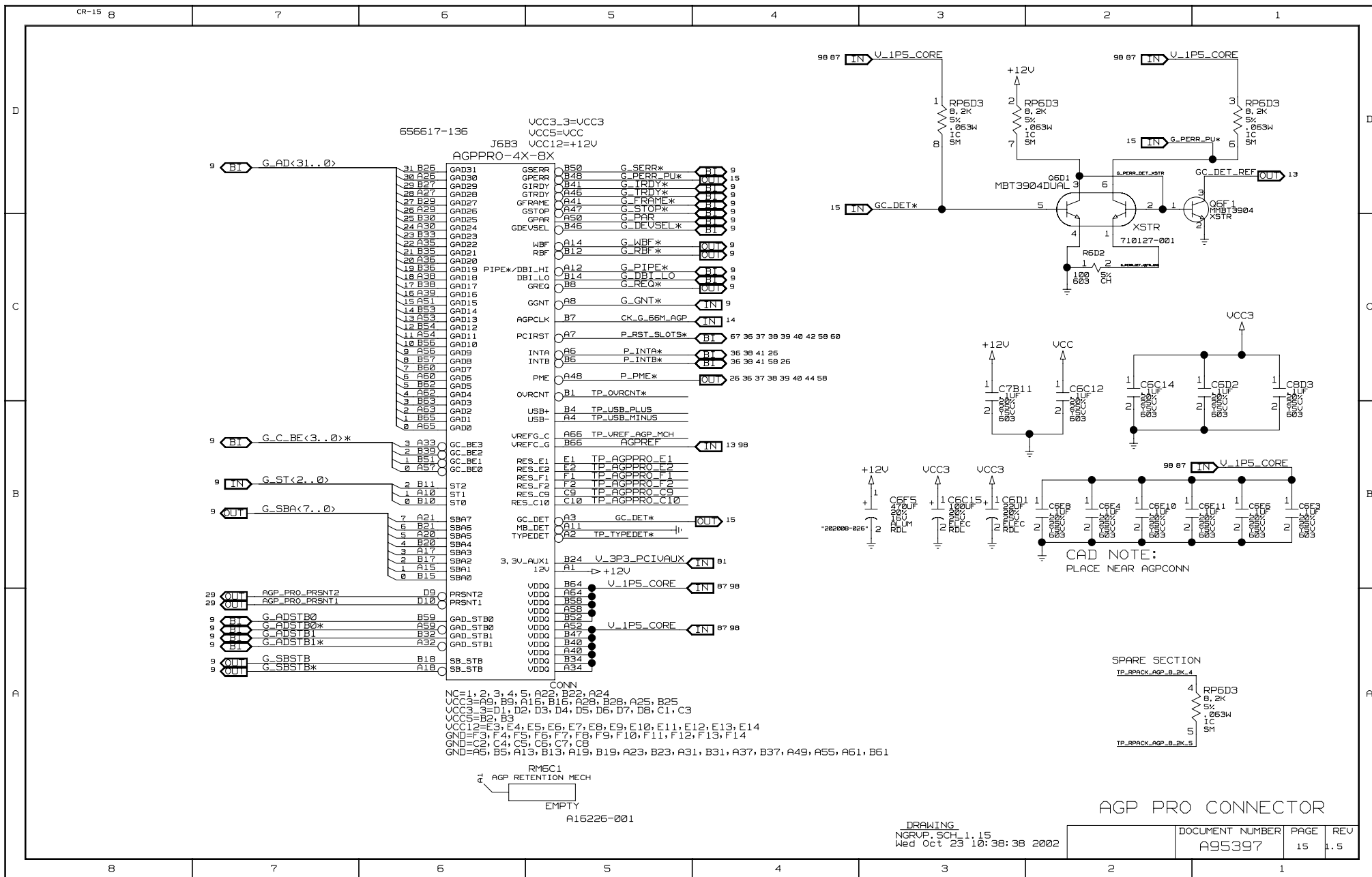




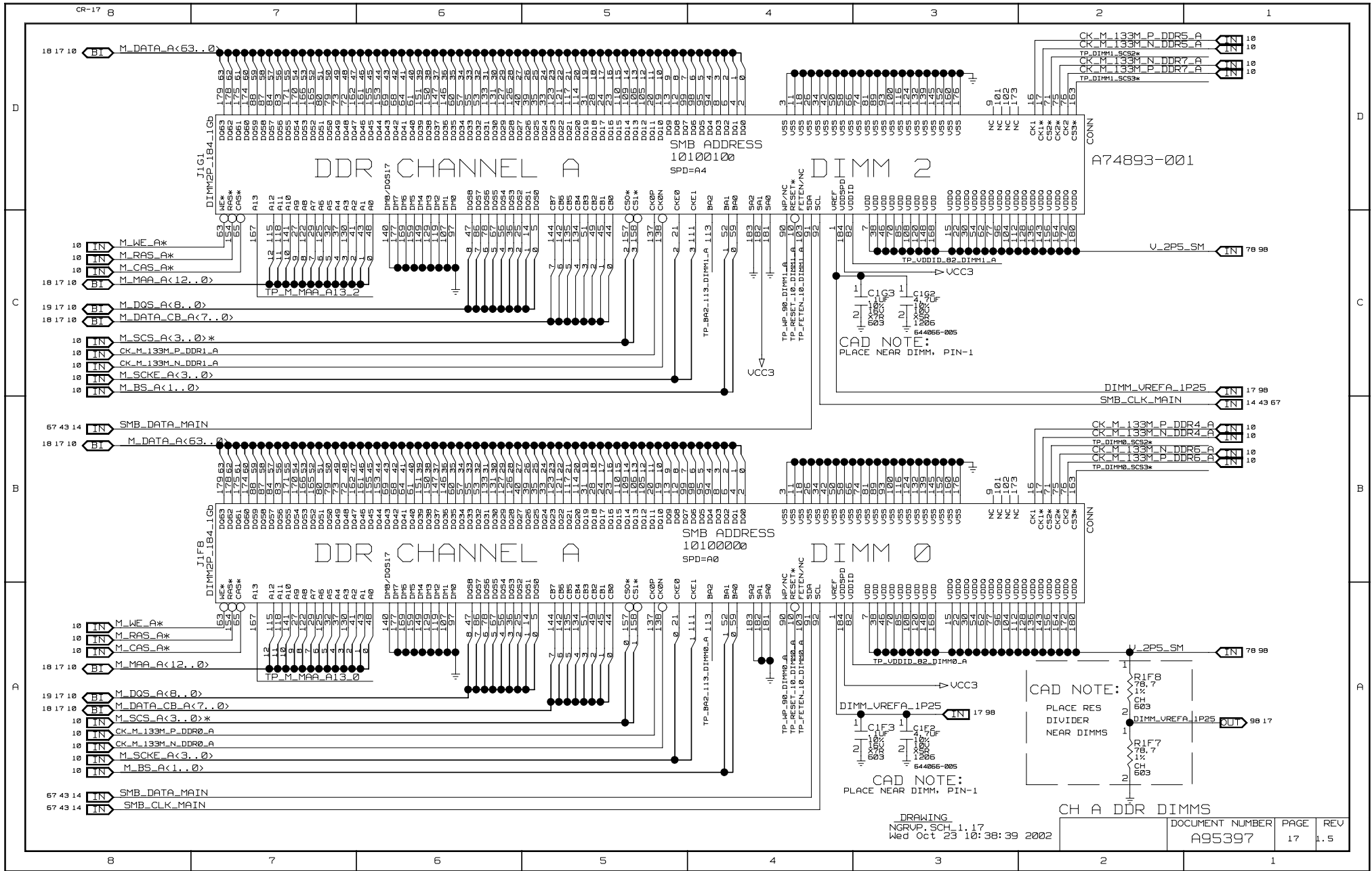


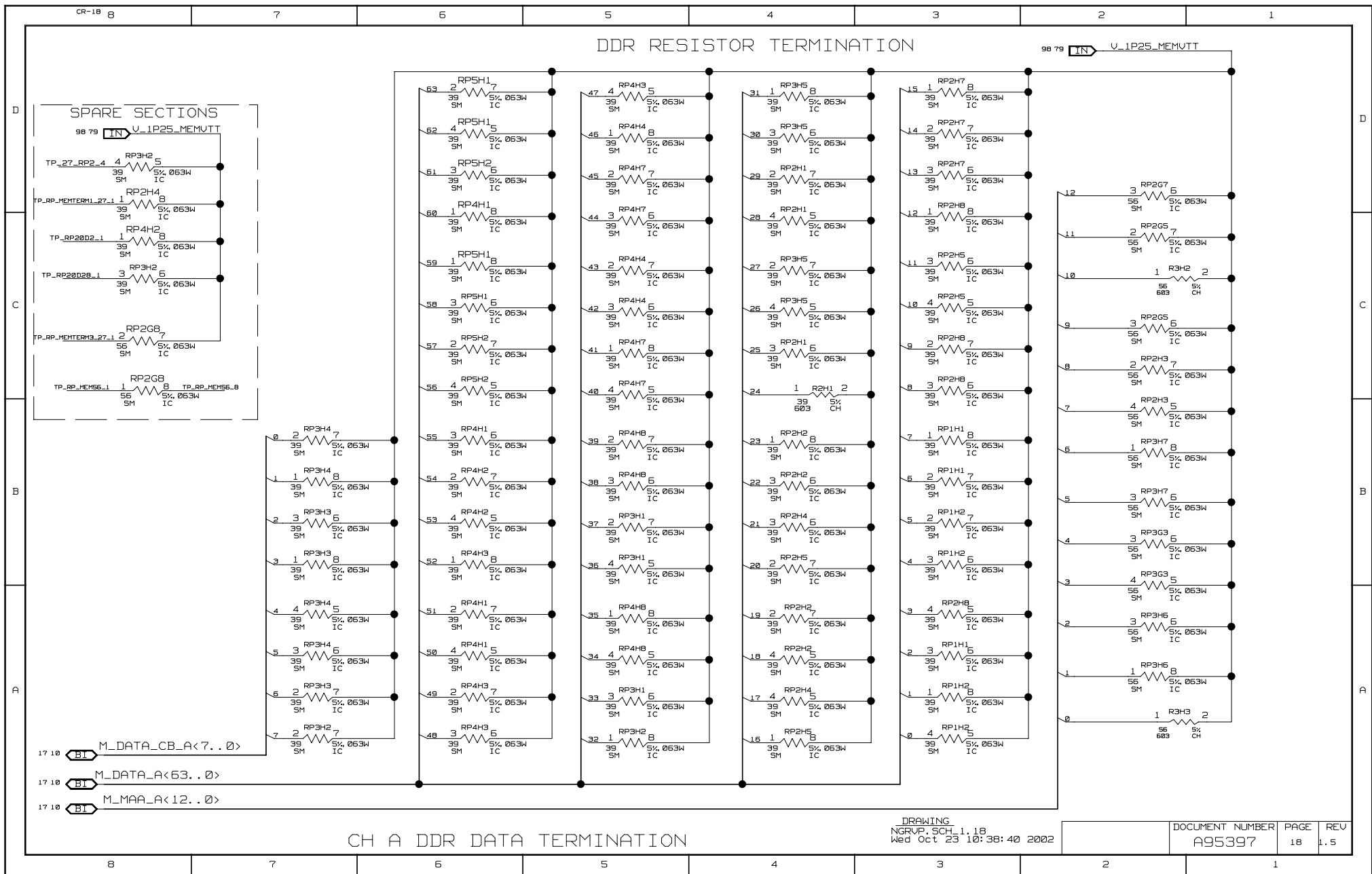


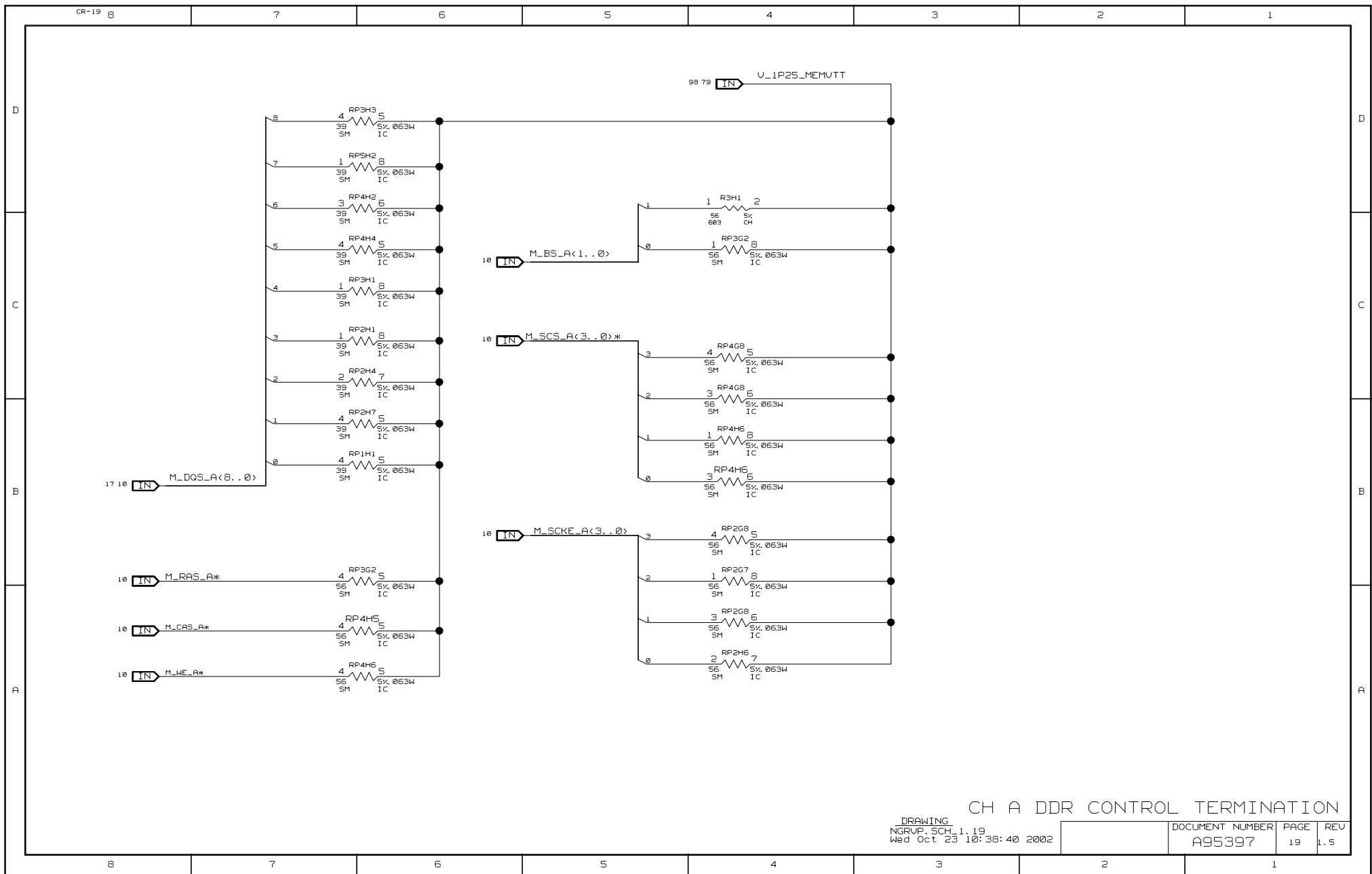


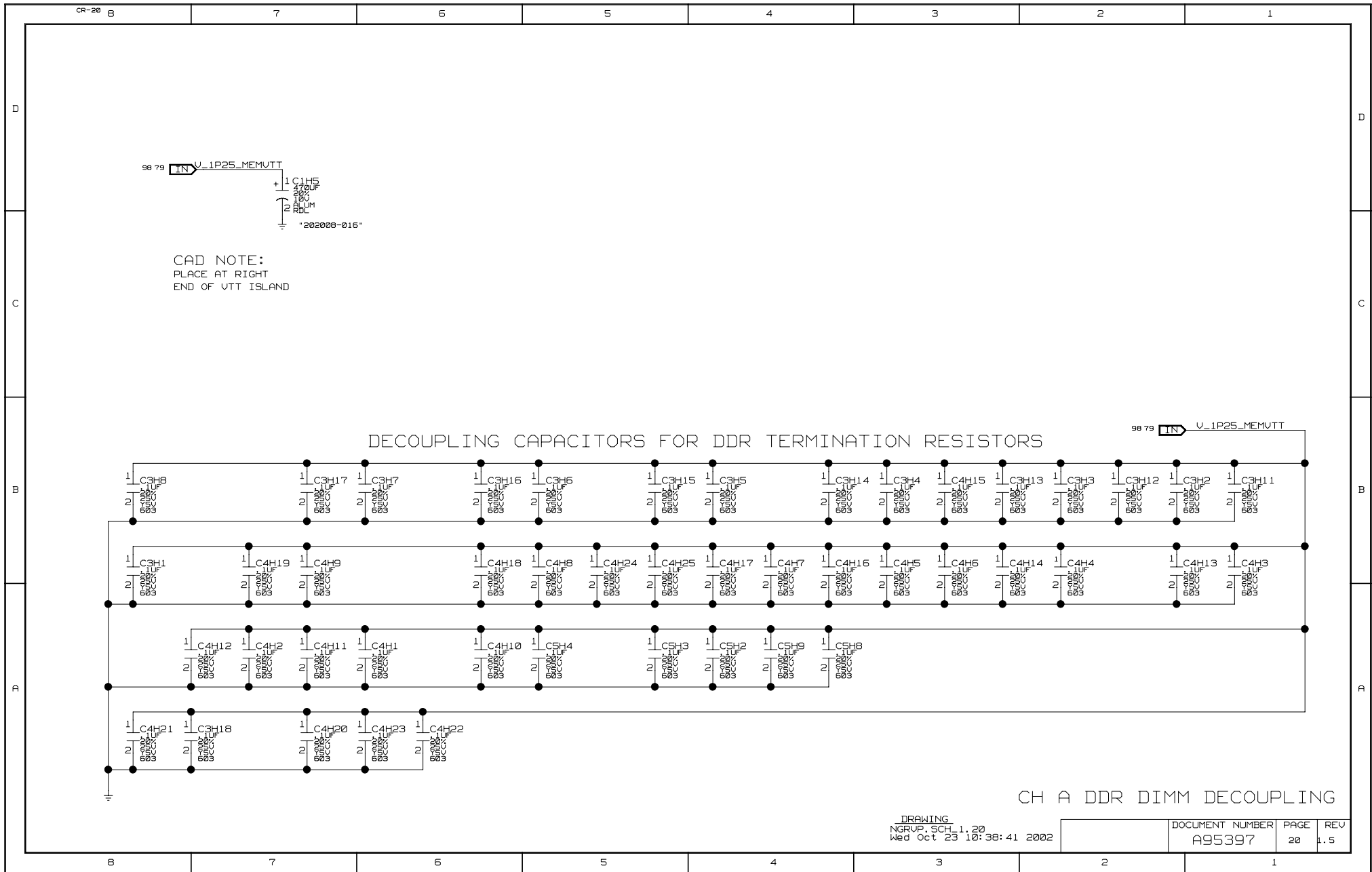


CR-16 8								7	6	5	4	3	2	1	
D	PAGE INTENTIONALLY BLANK														D
C															C
B															B
A															A
8								7	6	5	4	3	2	1	
DRAWING NGRUP.SCH_1.16 Wed Oct 23 10:38:38 2002												DOCUMENT NUMBER A95397		PAGE 16	REV 1.5









CR-21 8

7

6

5

4

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2

1

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C

C

B

B

A

A

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NGRVP.SCH_1.21
Wed Oct 23 10:38:41 2002

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A95397	21	1.5

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6

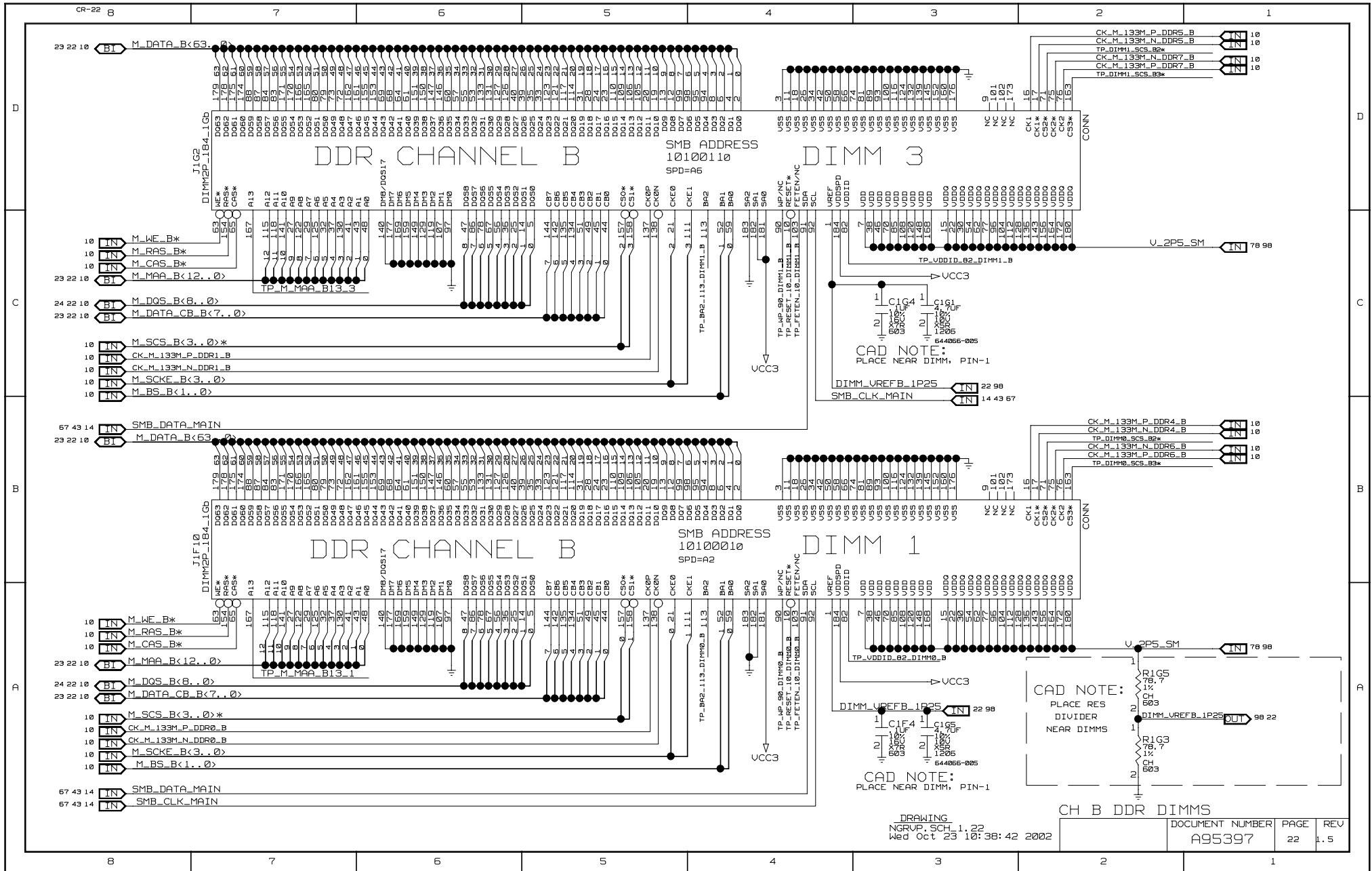
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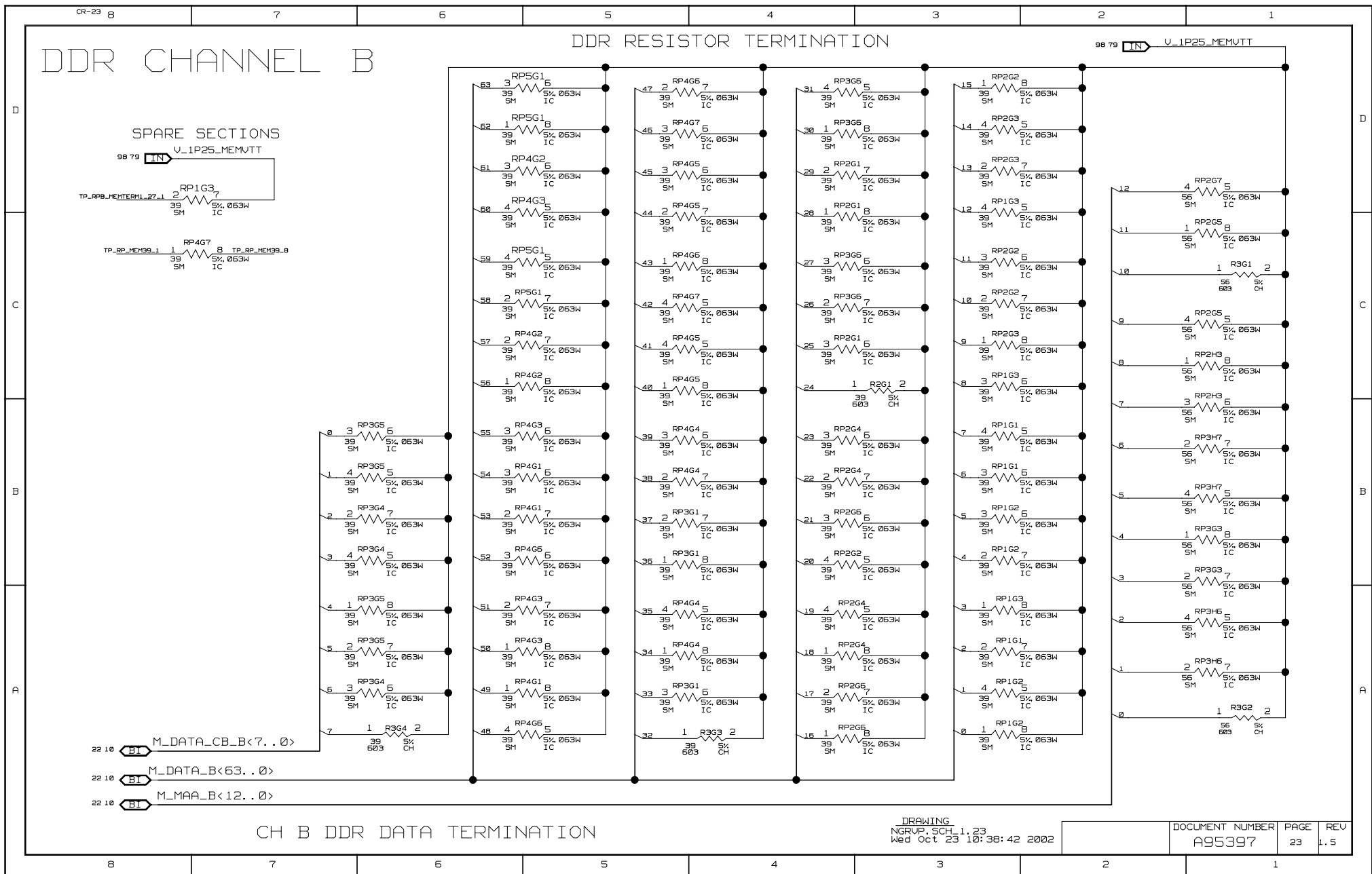
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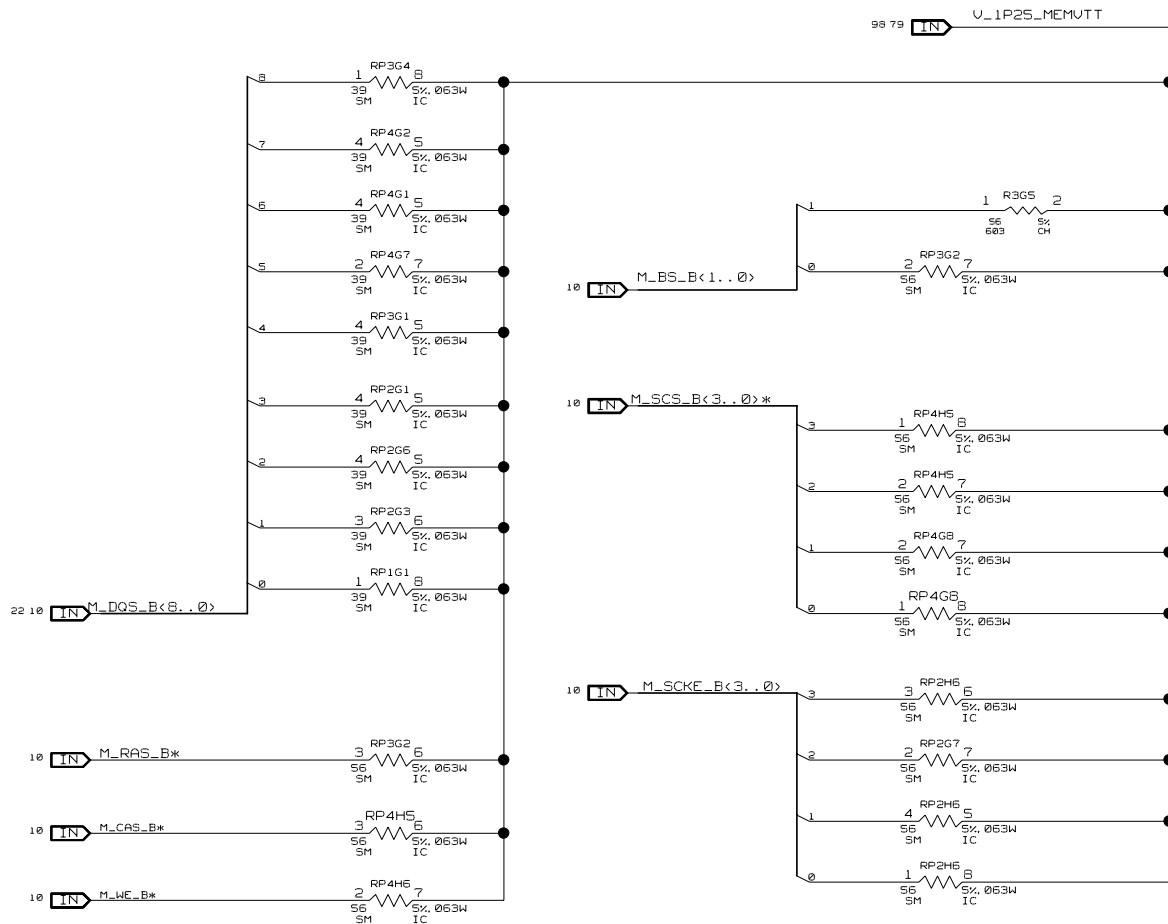
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DDR CHANNEL B

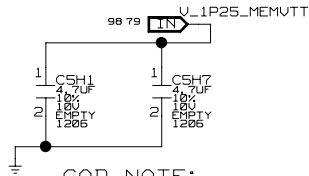


CH B DDR CONTROL TERMINATION

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NGRUP: SCH_1.24
Wed Oct 23 10:38:43 2002

DOCUMENT NUMBER	PAGE	REV
A95397	24	1.5

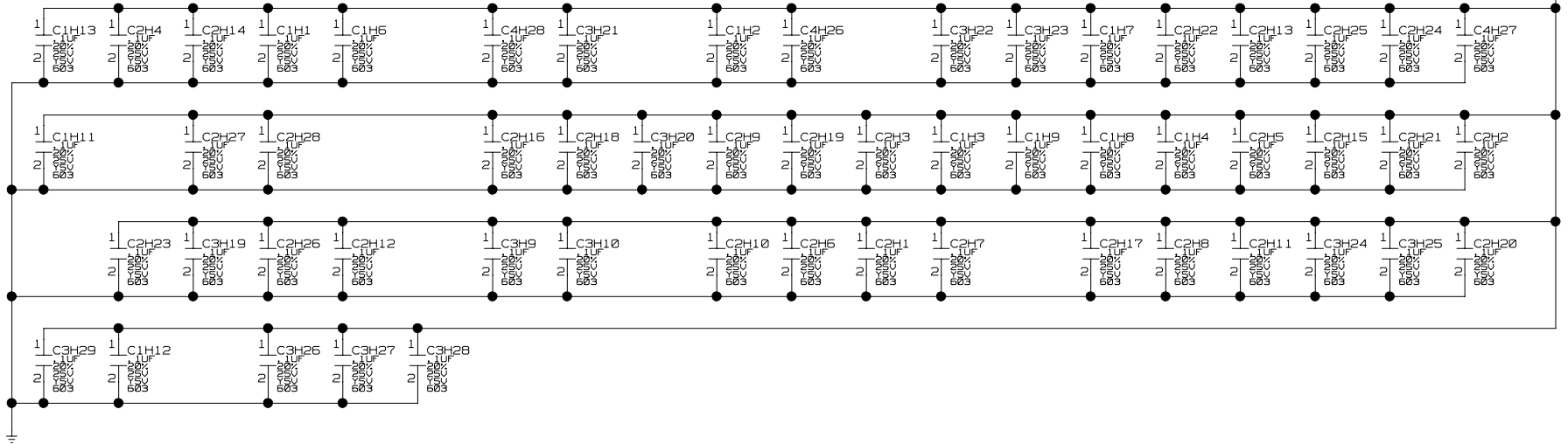
DDR CHANNEL B



CAD NOTE:
PLACED AT LEFT
END OF VTT ISLAND

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

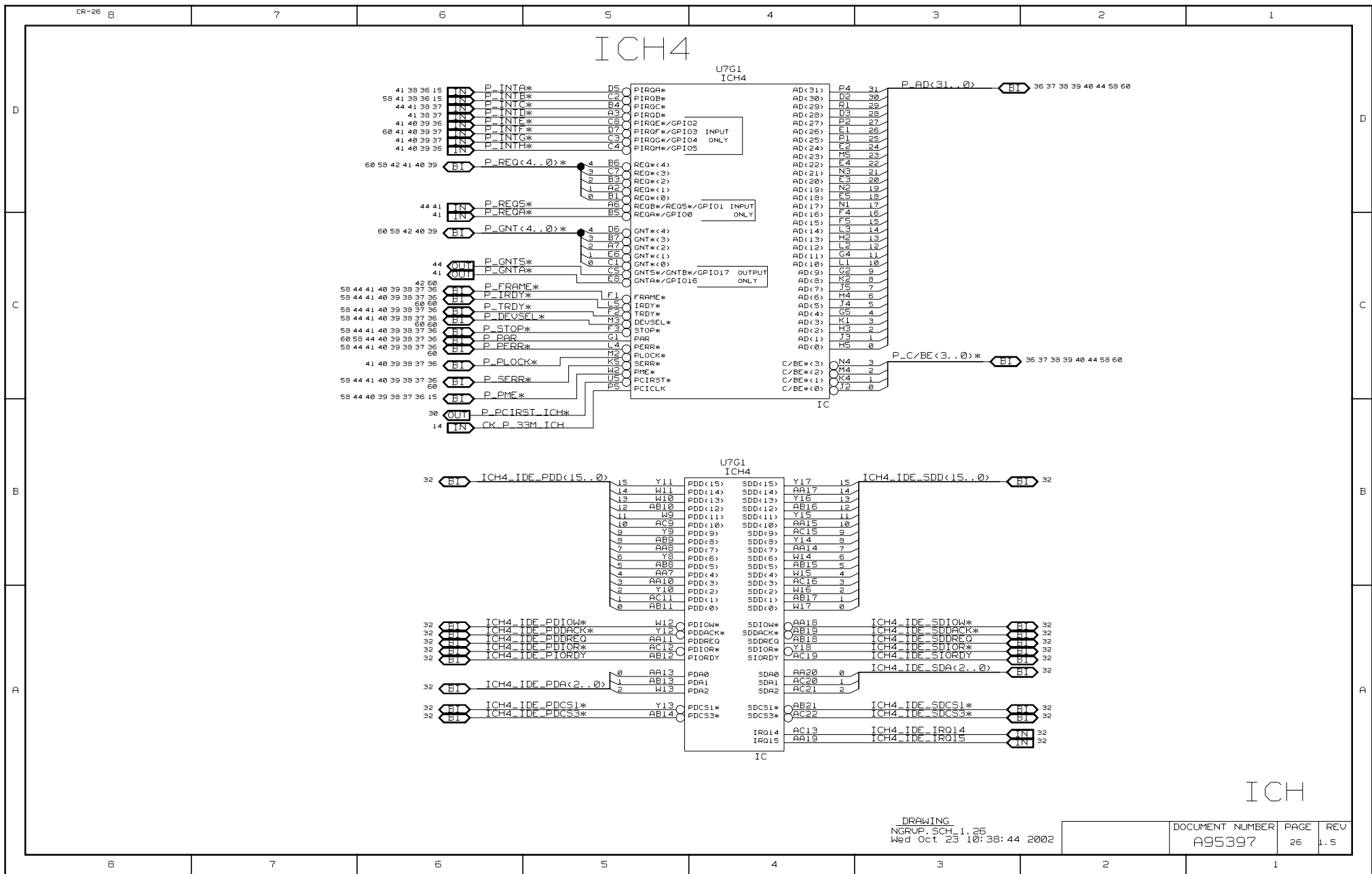
98 79 1N U_1P25_MEMVTT

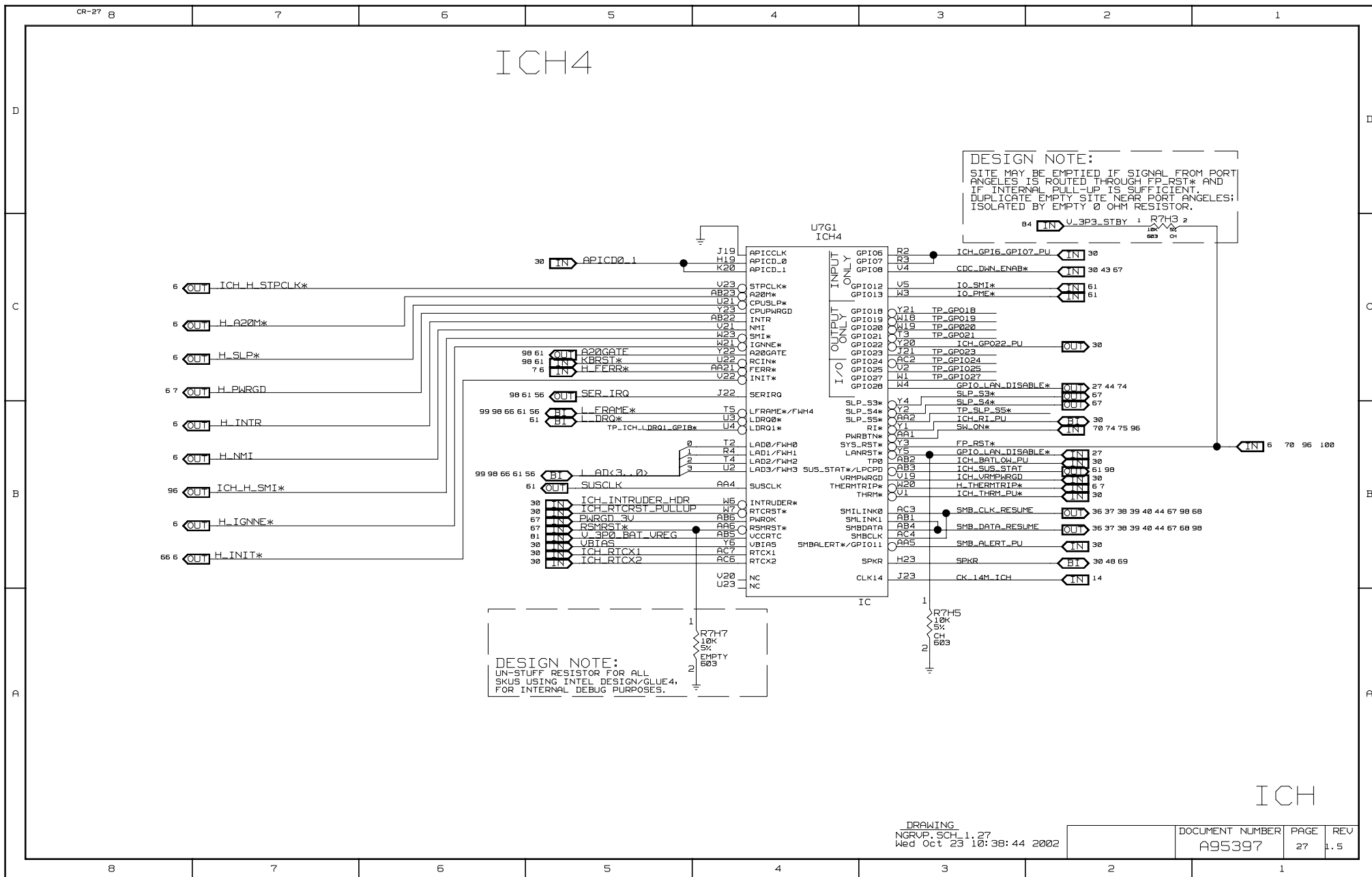


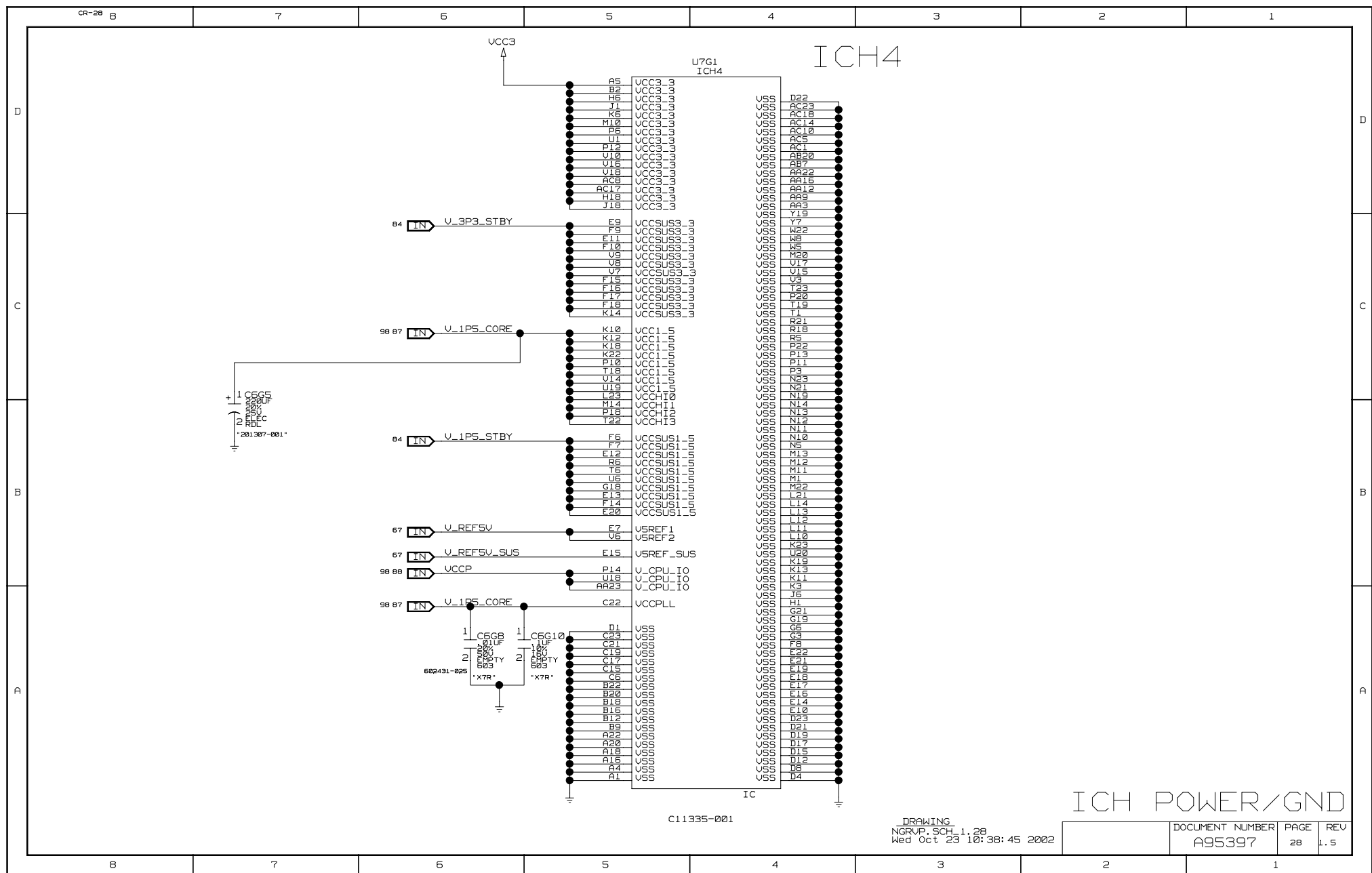
CH B DDR DIMM DECOUPLING

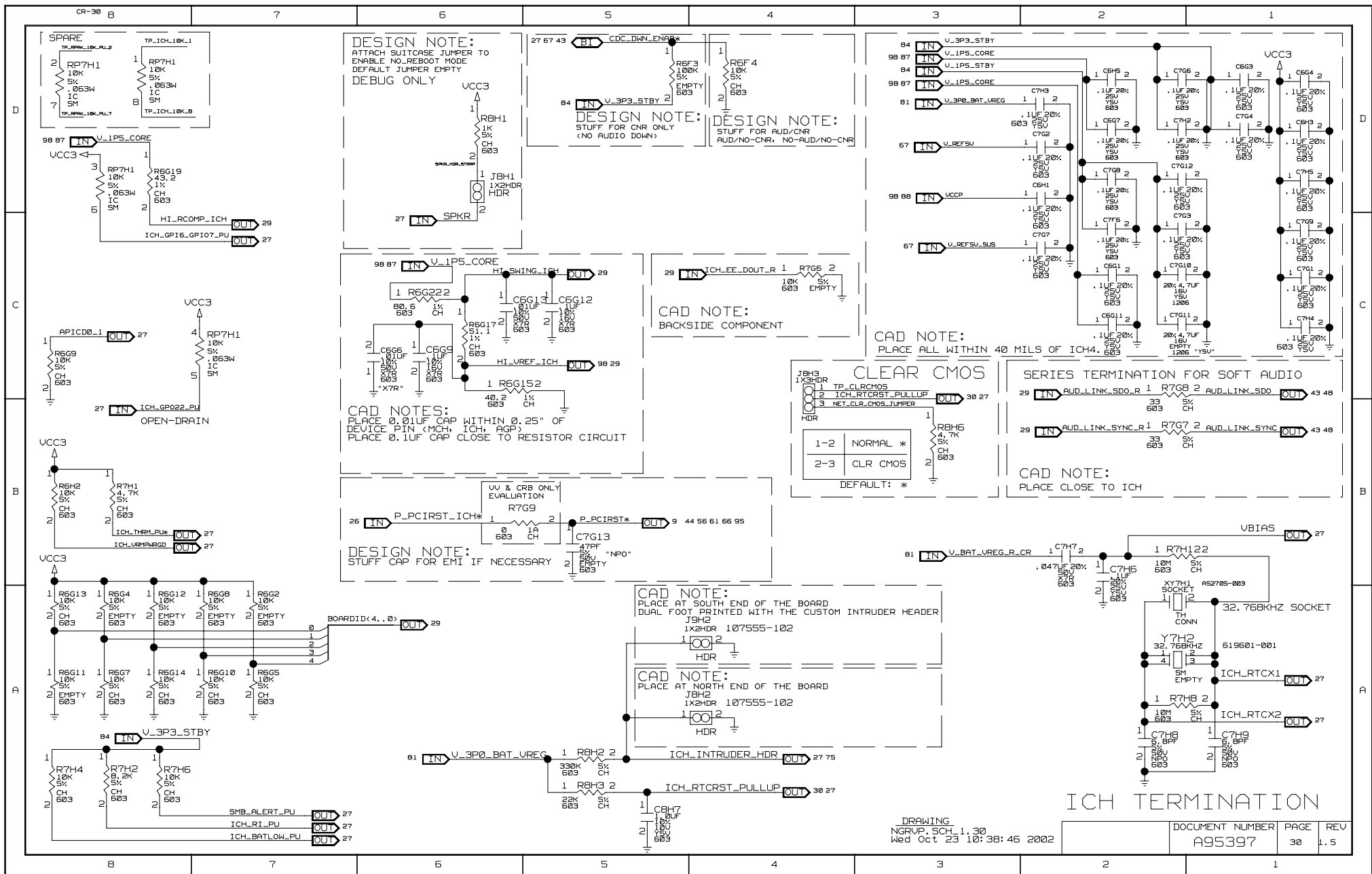
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NGRUP.SCH_1.25
Wed Oct 23 10:38:43 2002

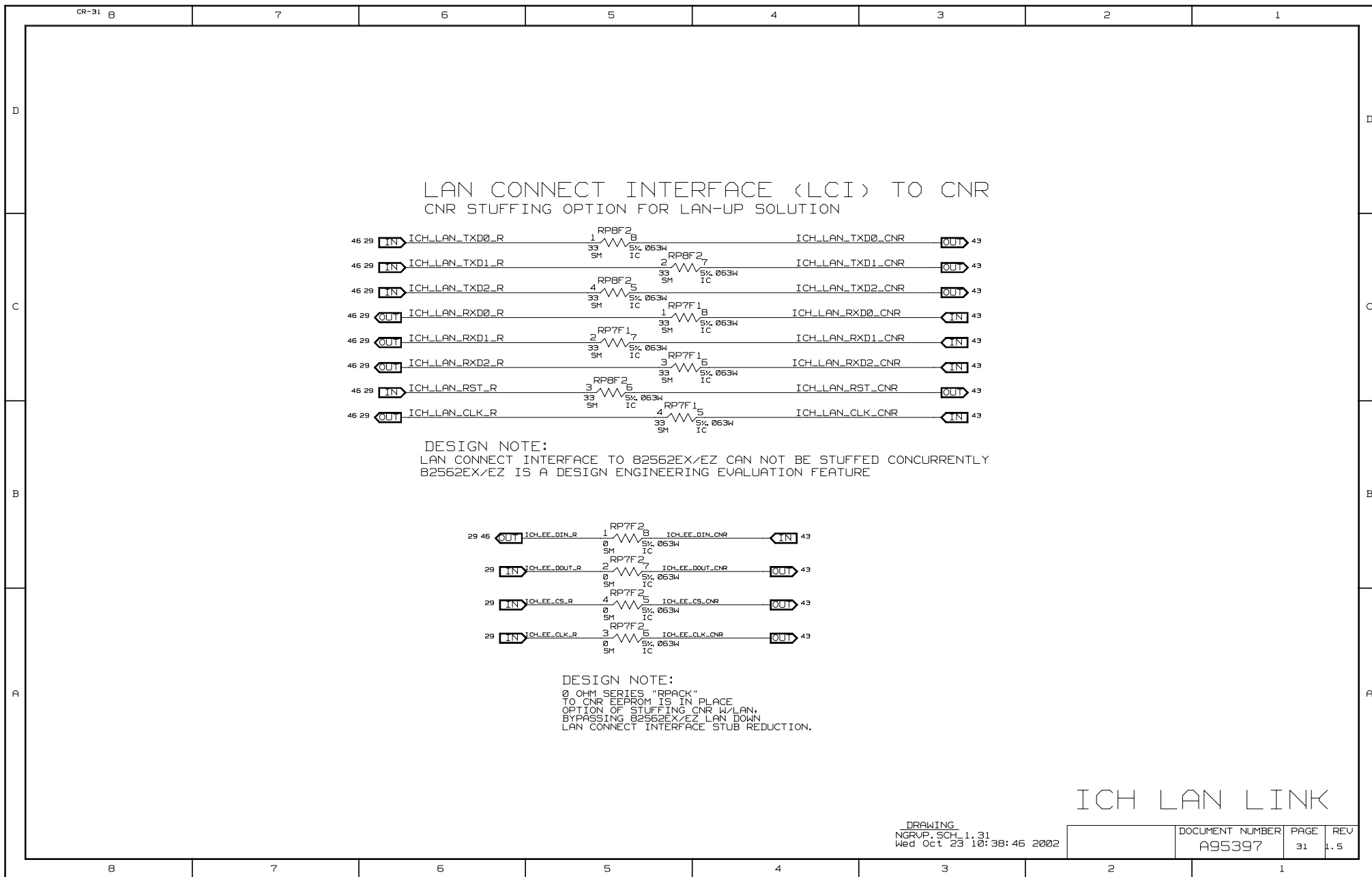
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A95397	25	1.5











DESIGN NOTE:

0 OHM SERIES "RPACK"

TO CNR EEPROM IS IN PLACE

OPTION OF STUFFING CNR W/LAN,

BYPASSING 82562EX/EZ LAN DOWN

LAN CONNECT INTERFACE STUB REDUCTION.

ICH LAN LINK

DRAWING

NGRUP.SCH_1.31

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A95397

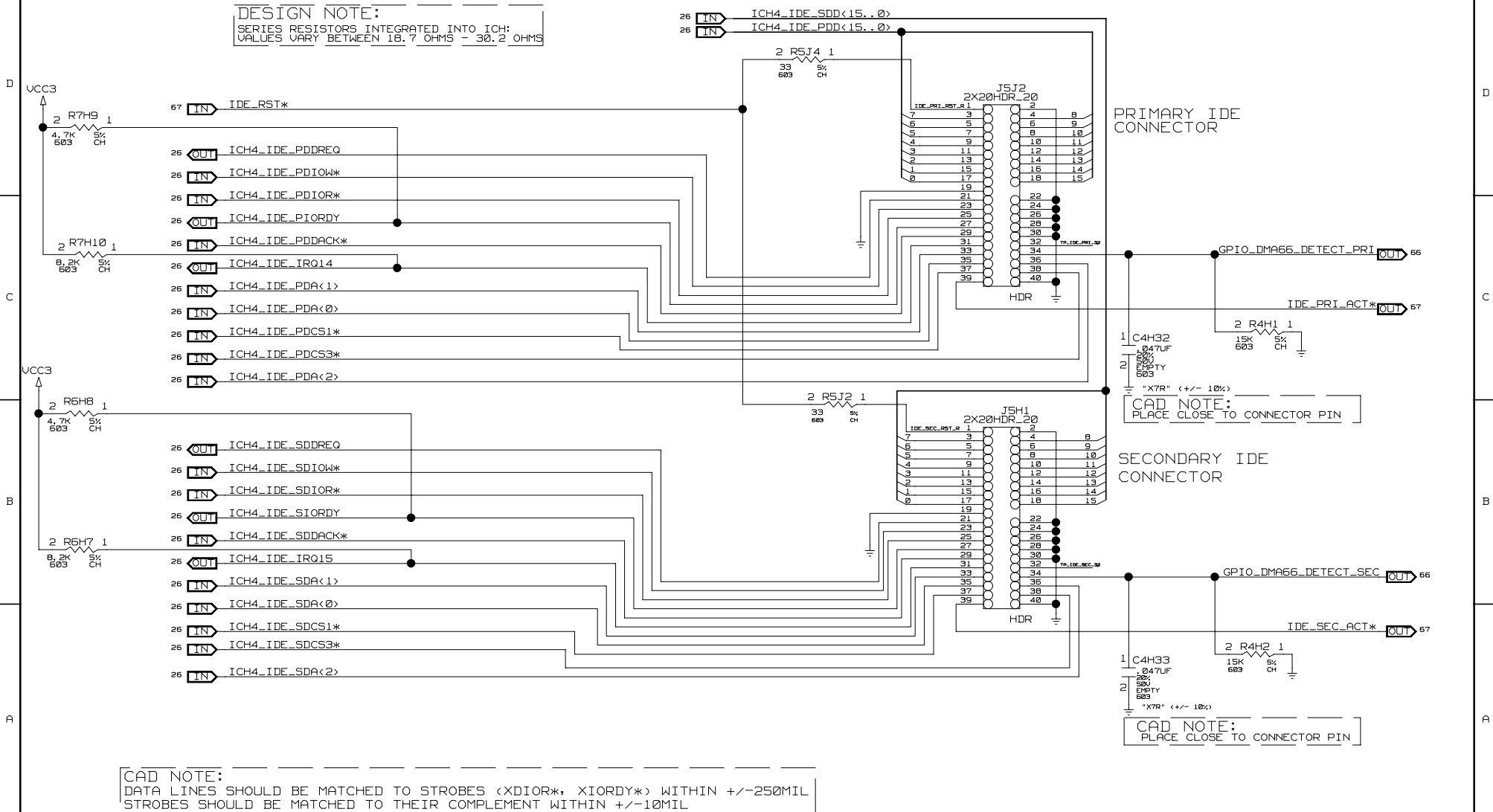
PAGE

31

REV

1.5

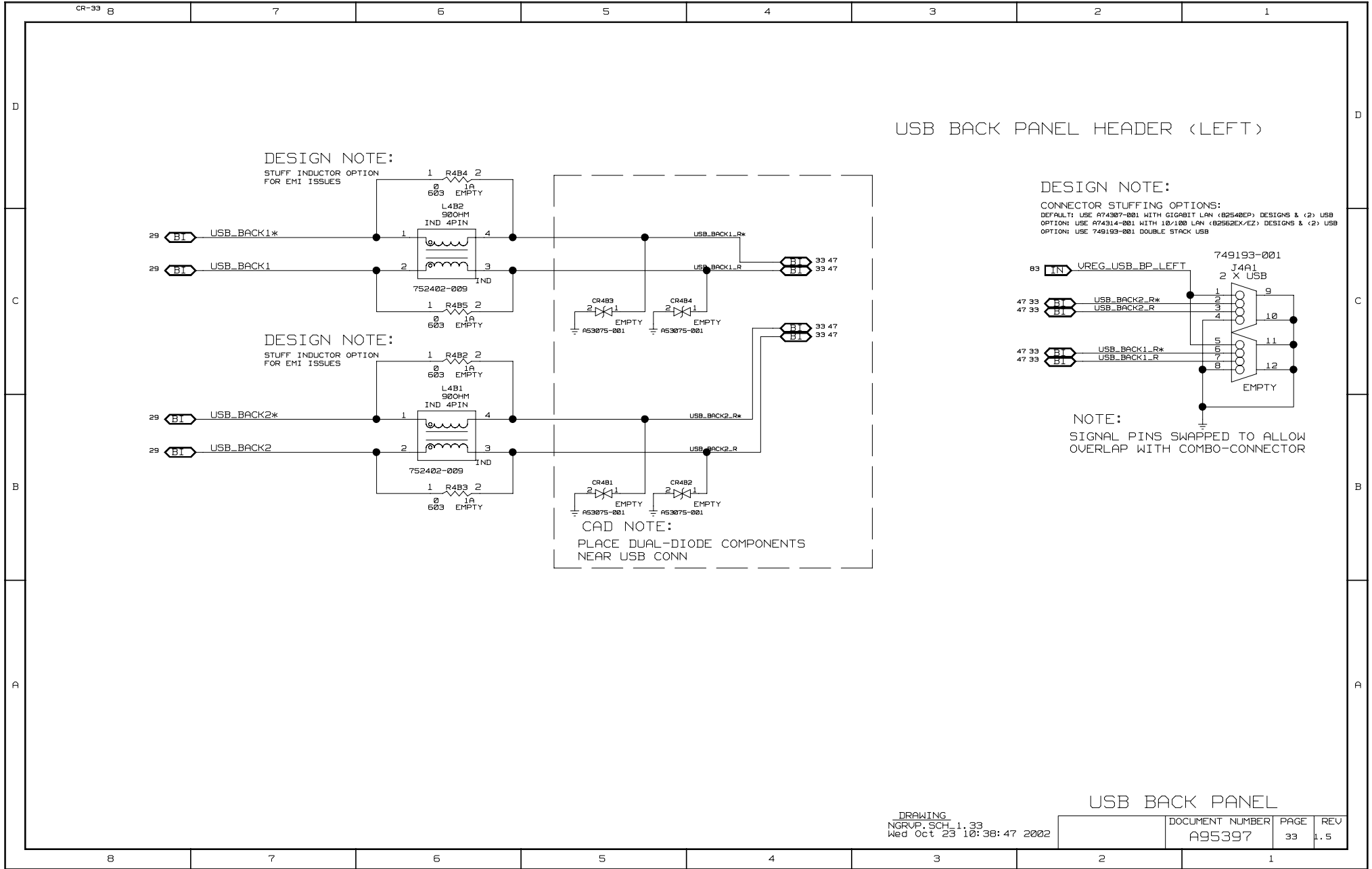
DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

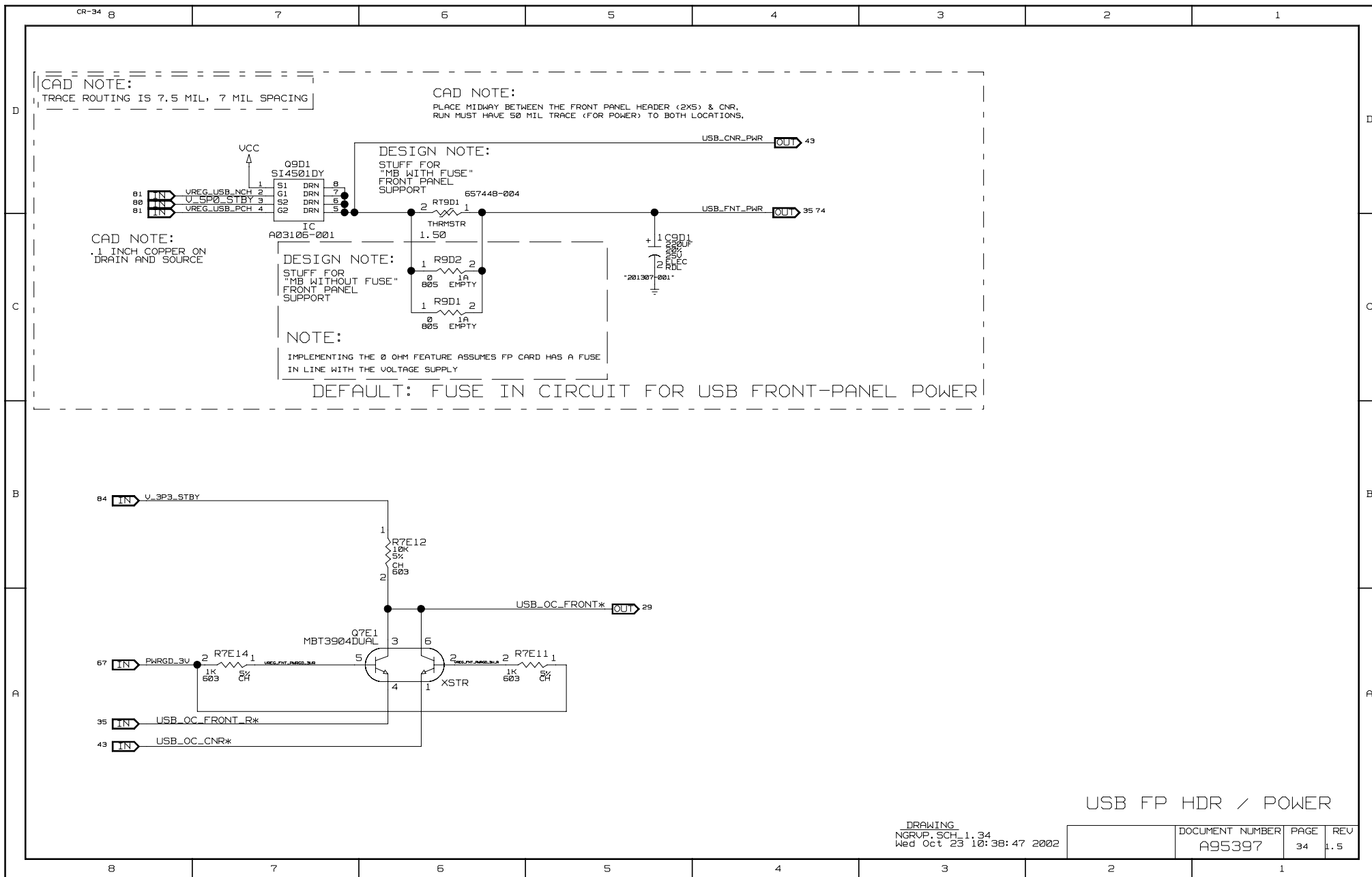


IDE CONNECTORS

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NGRUP_SCH_1.32
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A95397	32	1.5





CAD NOTE:
TRACE ROUTING IS 7.5 MIL, 7 MIL SPACING

CAD NOTE:
PLACE MIDWAY BETWEEN THE FRONT PANEL HEADER (2X5) & CNR.
RUN MUST HAVE 50 MIL TRACE (FOR POWER) TO BOTH LOCATIONS.

DESIGN NOTE:
STUFF FOR "MB WITH FUSE"
FRONT PANEL SUPPORT

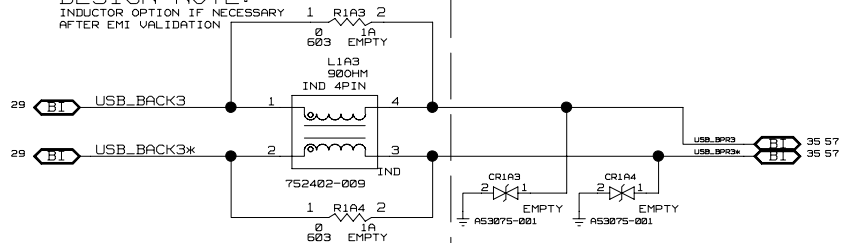
DESIGN NOTE:
STUFF FOR "MB WITHOUT FUSE"
FRONT PANEL SUPPORT

NOTE:
IMPLEMENTING THE 0 OHM FEATURE ASSUMES FP CARD HAS A FUSE
IN LINE WITH THE VOLTAGE SUPPLY

DEFAULT: FUSE IN CIRCUIT FOR USB FRONT-PANEL POWER

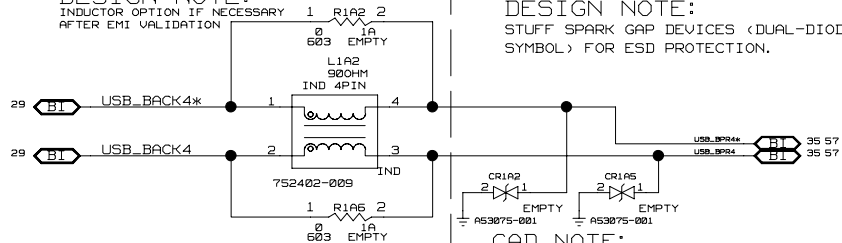
DESIGN NOTE:

INDUCTOR OPTION IF NECESSARY
AFTER EMI VALIDATION



DESIGN NOTE:

INDUCTOR OPTION IF NECESSARY
AFTER EMI VALIDATION



DESIGN NOTE:

STUFF SPARK GAP DEVICES (DUAL-DIODE
SYMBOL) FOR ESD PROTECTION.

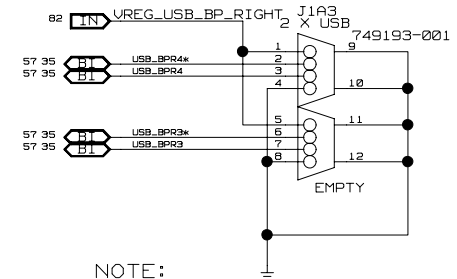
CAD NOTE:

PLACE DUAL-DIODE COMPONENTS
NEAR USB CONN

USB BACK PANEL HEADER (RIGHT)

DESIGN NOTE:

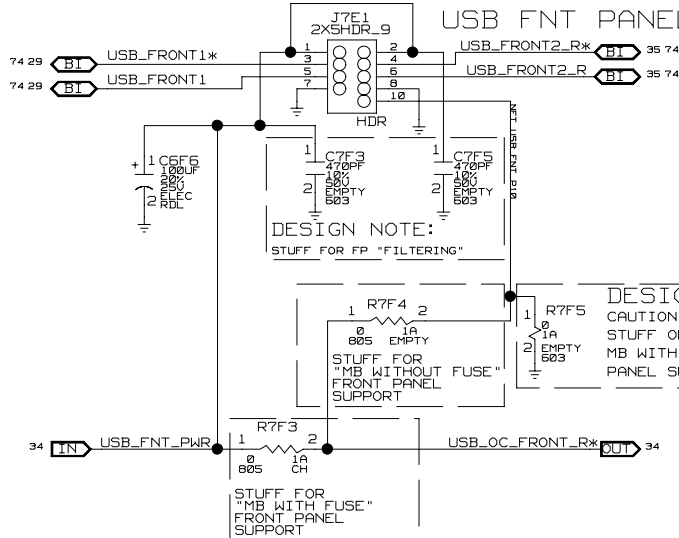
CONNECTOR STUFFING OPTIONS:
DEFAULT: USE A74325-001 WITH 1394 & (2) USB
OPTION: USE 749193-001 DOUBLE STACK USB



NOTE:

SIGNAL PINS SWAPPED TO ALLOW
OVERLAP WITH COMBO-CONNECTOR

USB FNT PANEL HEADER



DESIGN NOTE:

STUFF FOR FP "FILTERING"

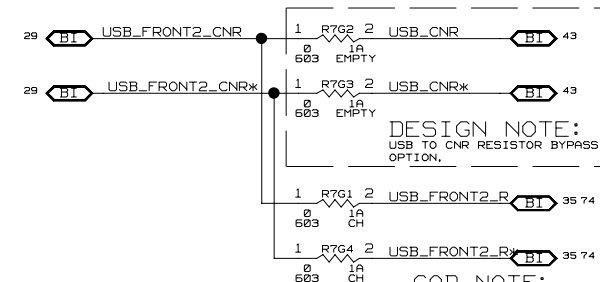
DESIGN NOTE:

CAUTION: 0 OHM TO GND.
STUFF ONLY FOR "CUSTOM
MB WITH FUSE" FRONT
PANEL SUPPORT

STUFF FOR
"MB WITHOUT FUSE"
FRONT PANEL
SUPPORT

STUFF FOR
"MB WITH FUSE"
FRONT PANEL
SUPPORT

USB SWITCH USB OPTION FOR CNR OR FRONT PANEL



DESIGN NOTE:

USB TO CNR RESISTOR BYPASS
OPTION.

CAD NOTE:
MINIMIZE STUBS TO 0.100 FOR
CNR AND FRONT PANEL HEADER

USB BPR / FP HDR

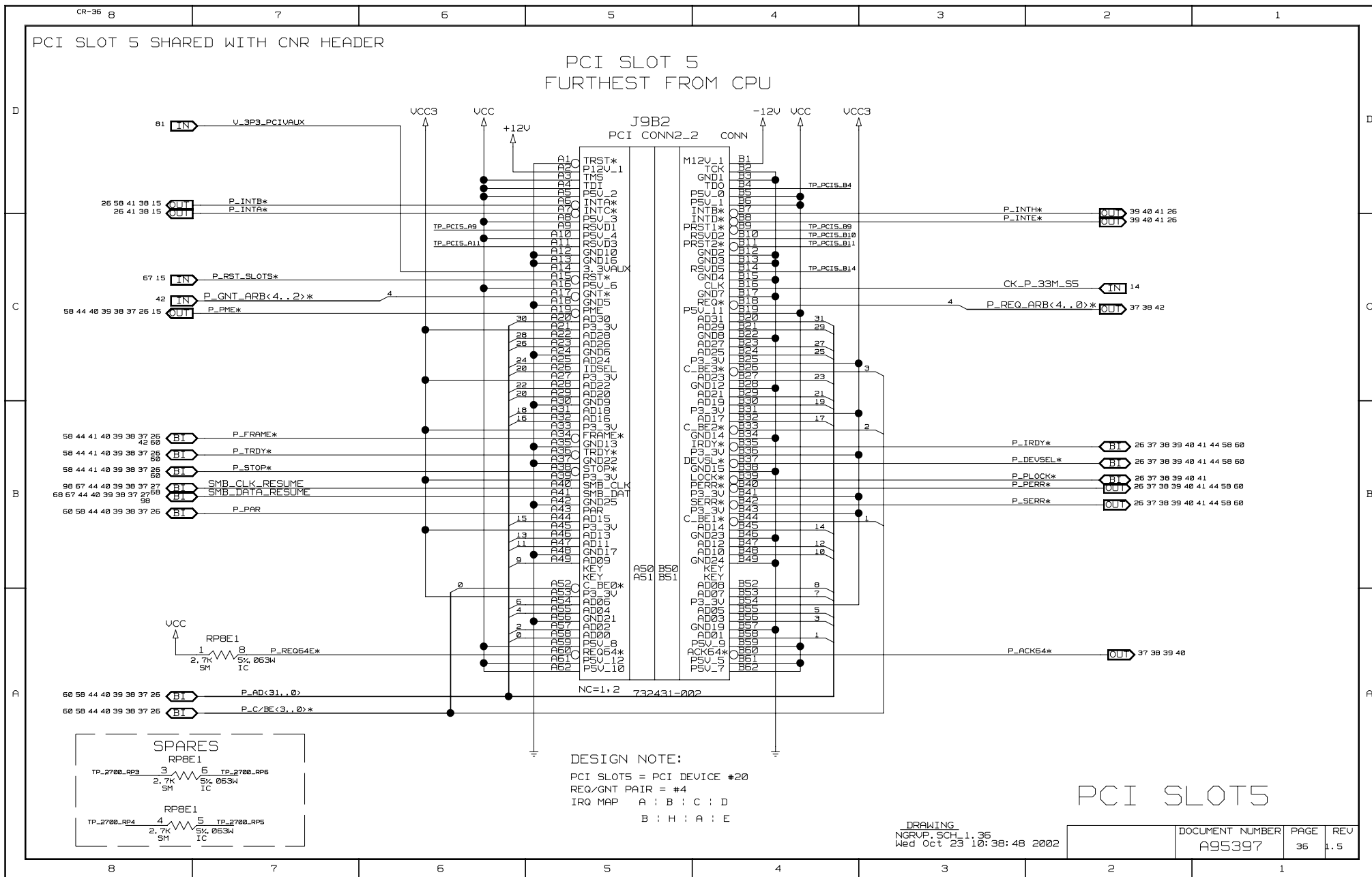
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NGRUP_SCH_1.35
Wed Oct 23 10:38:48 2002

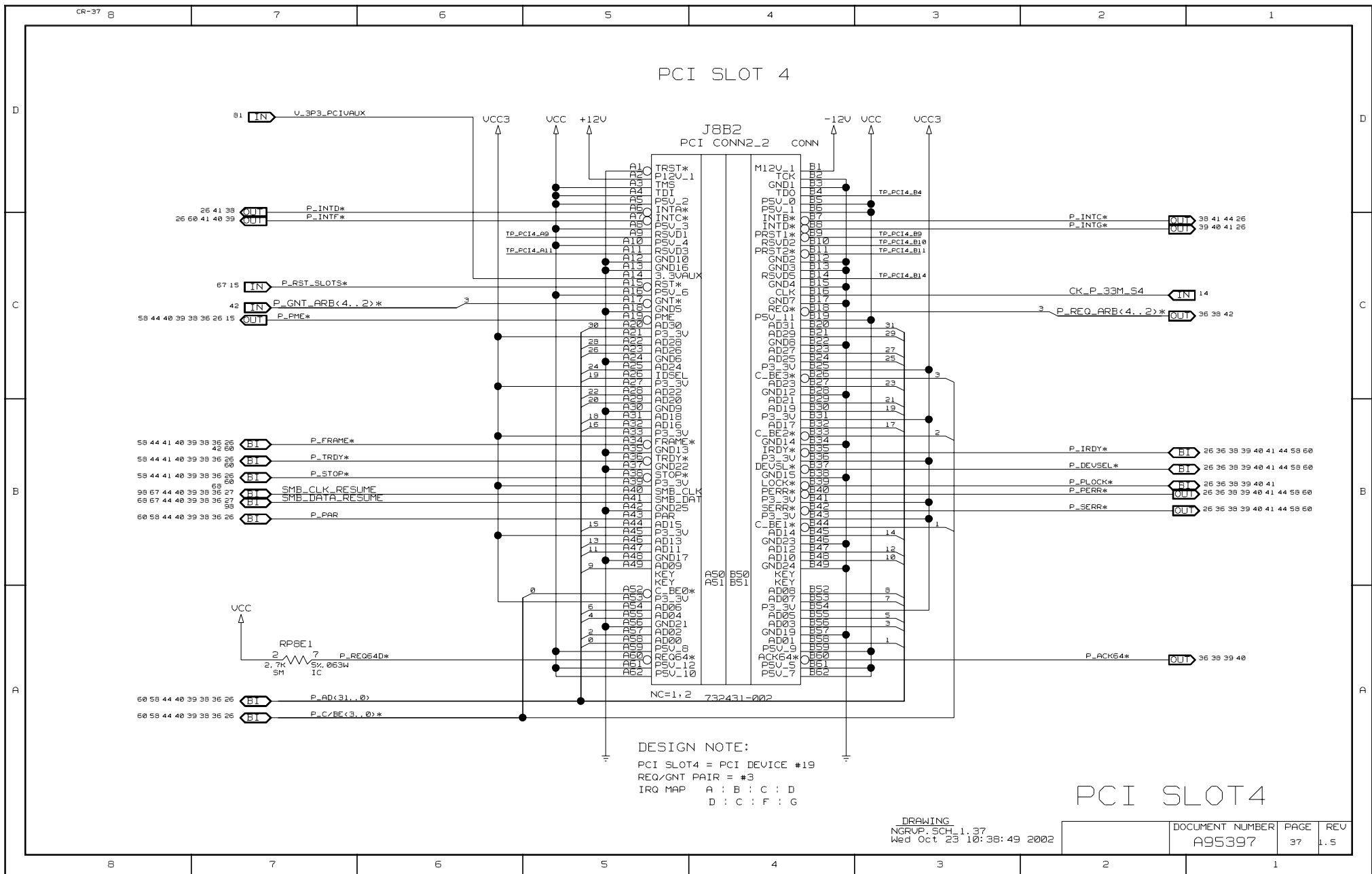
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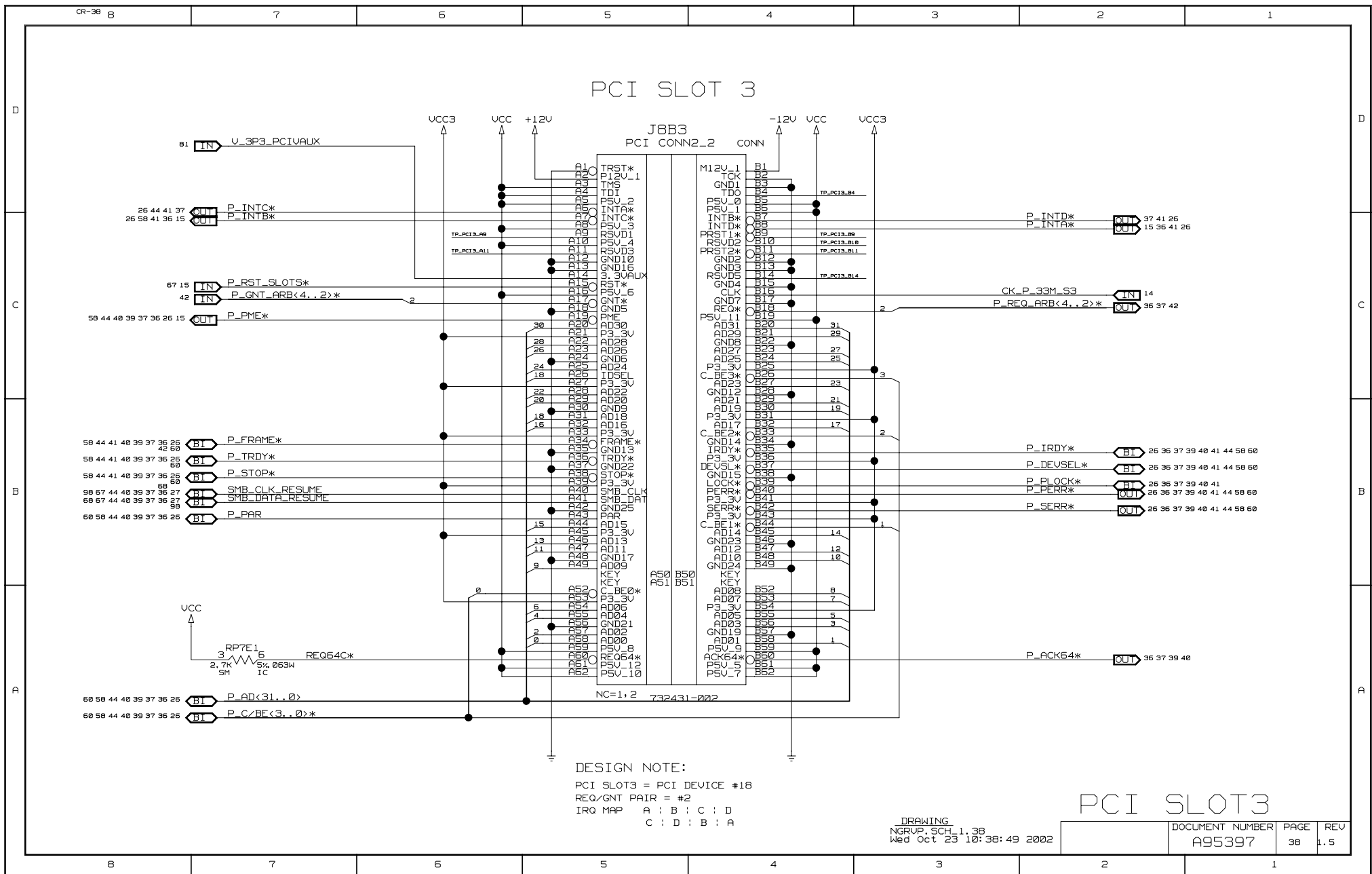
PAGE
35

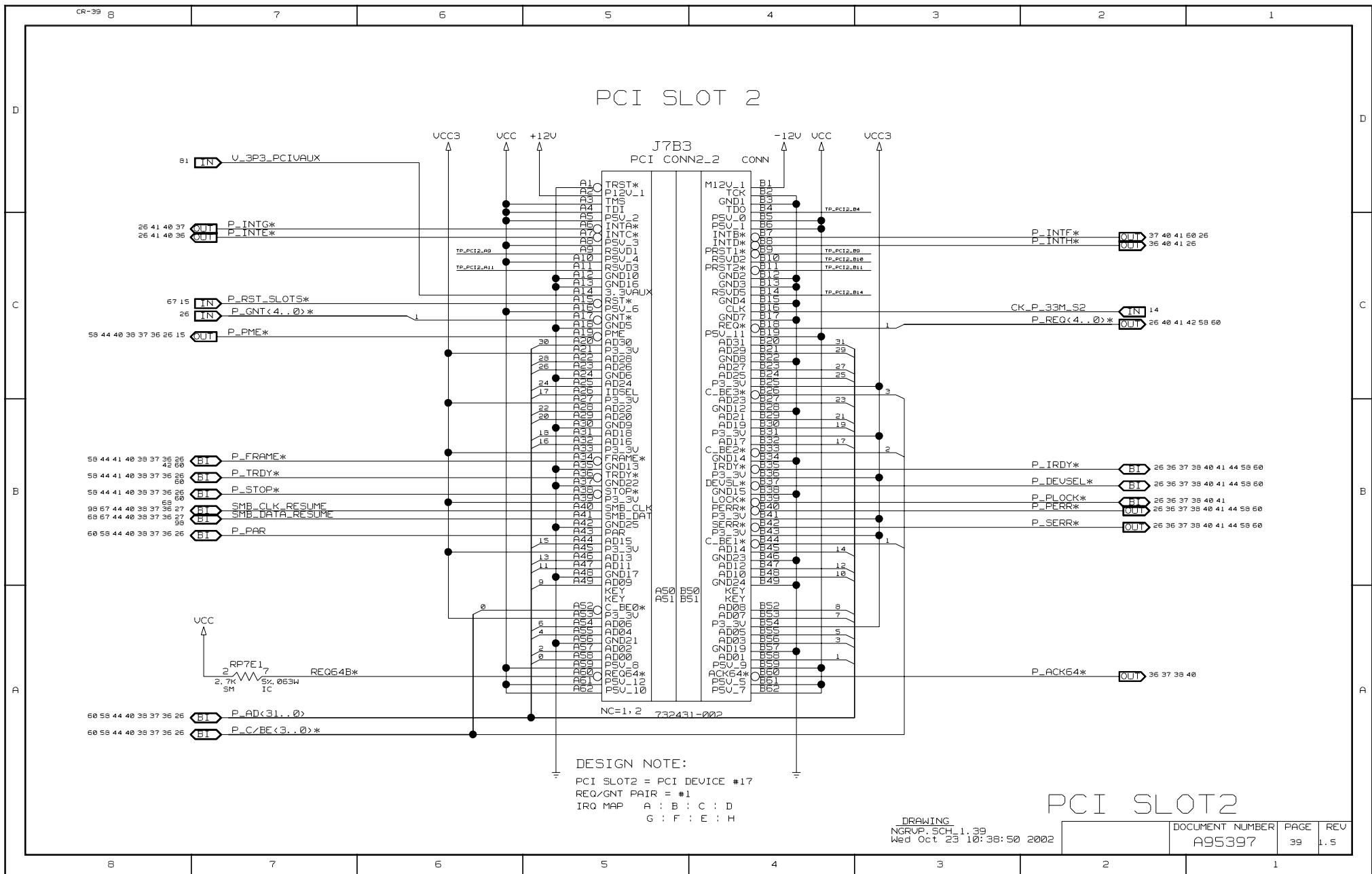
REV
1.5

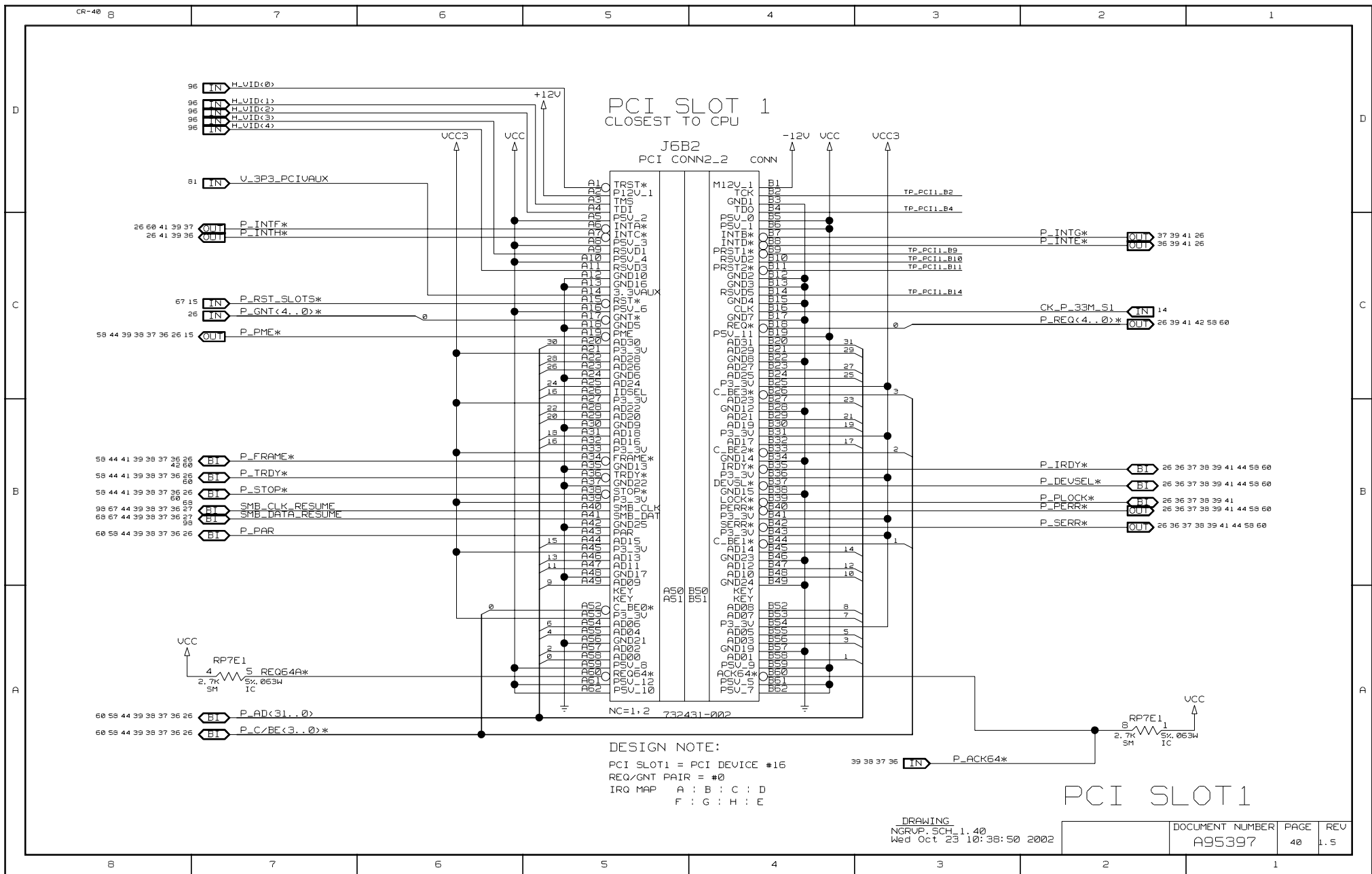
DEFAULT: FUSE IN CIRCUIT FOR USB FRONT-PANEL POWER

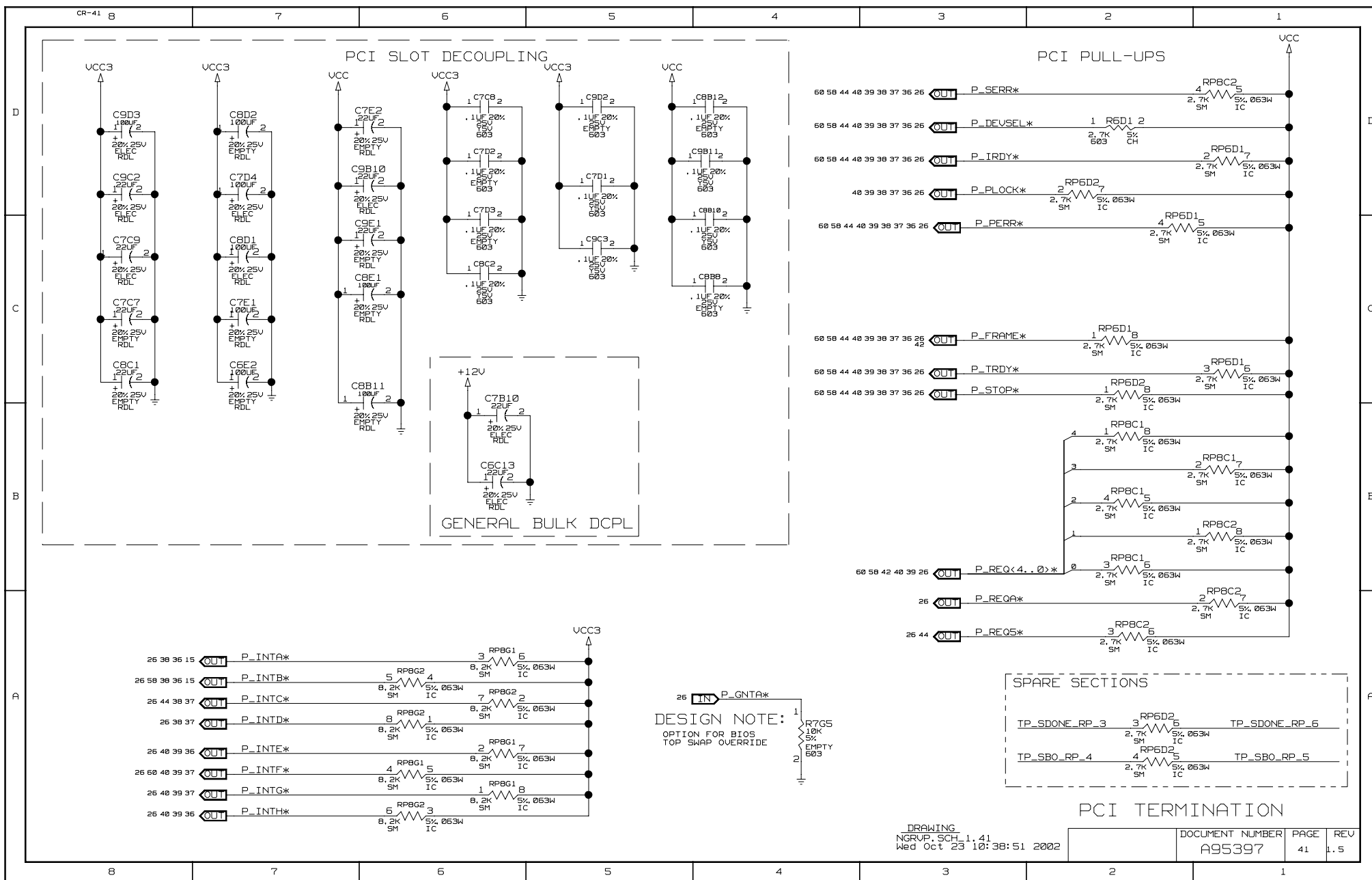


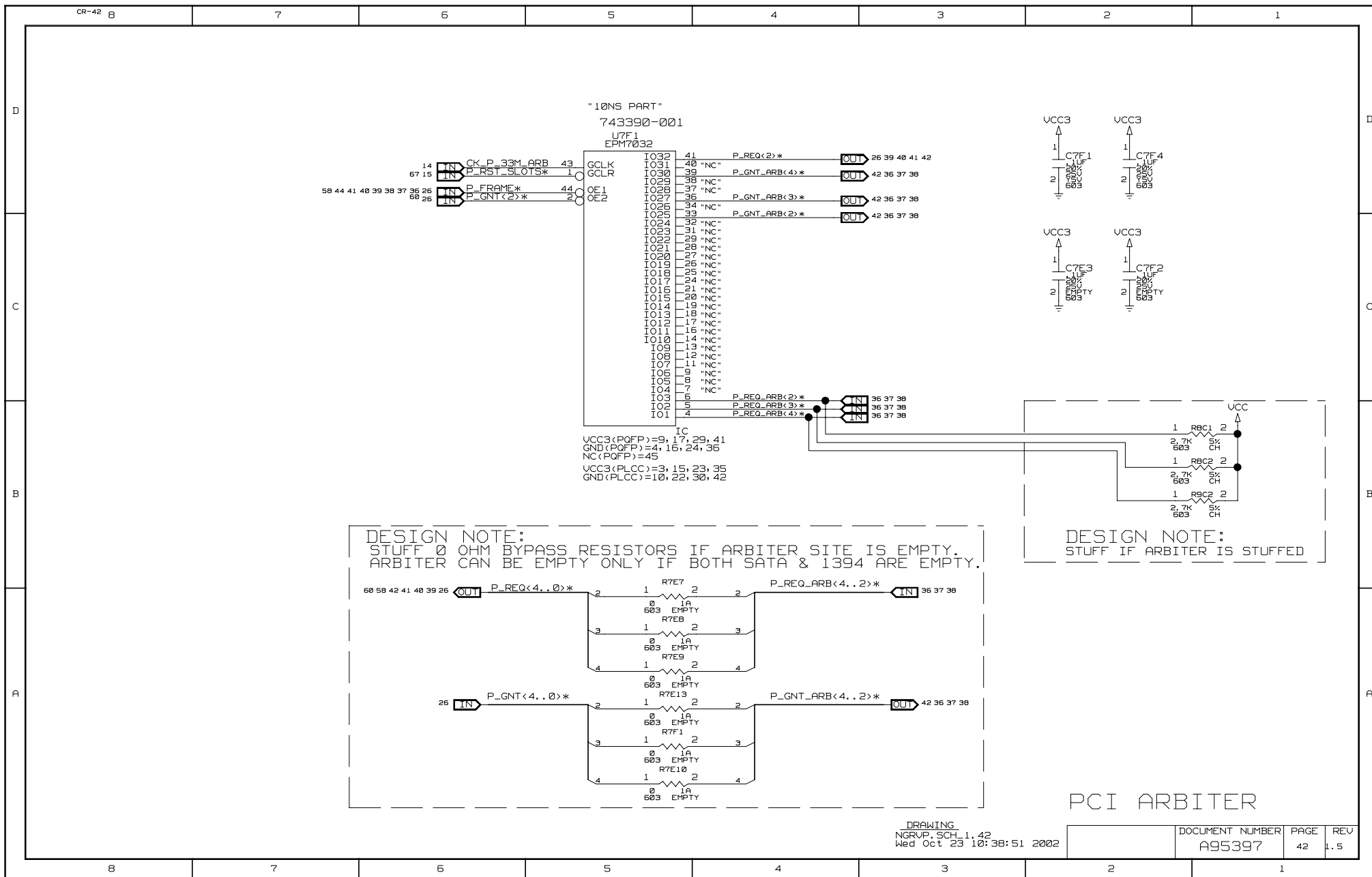


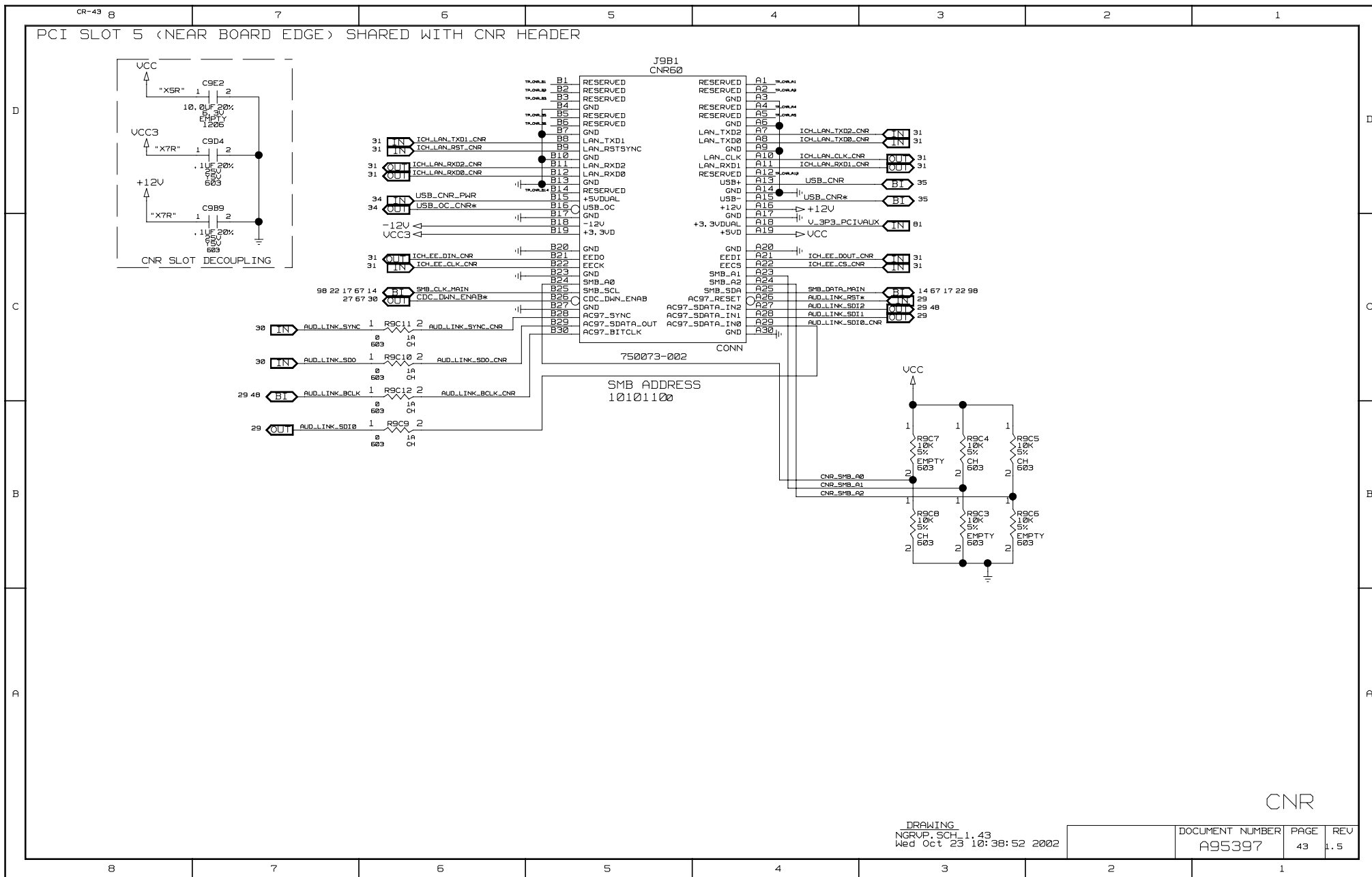


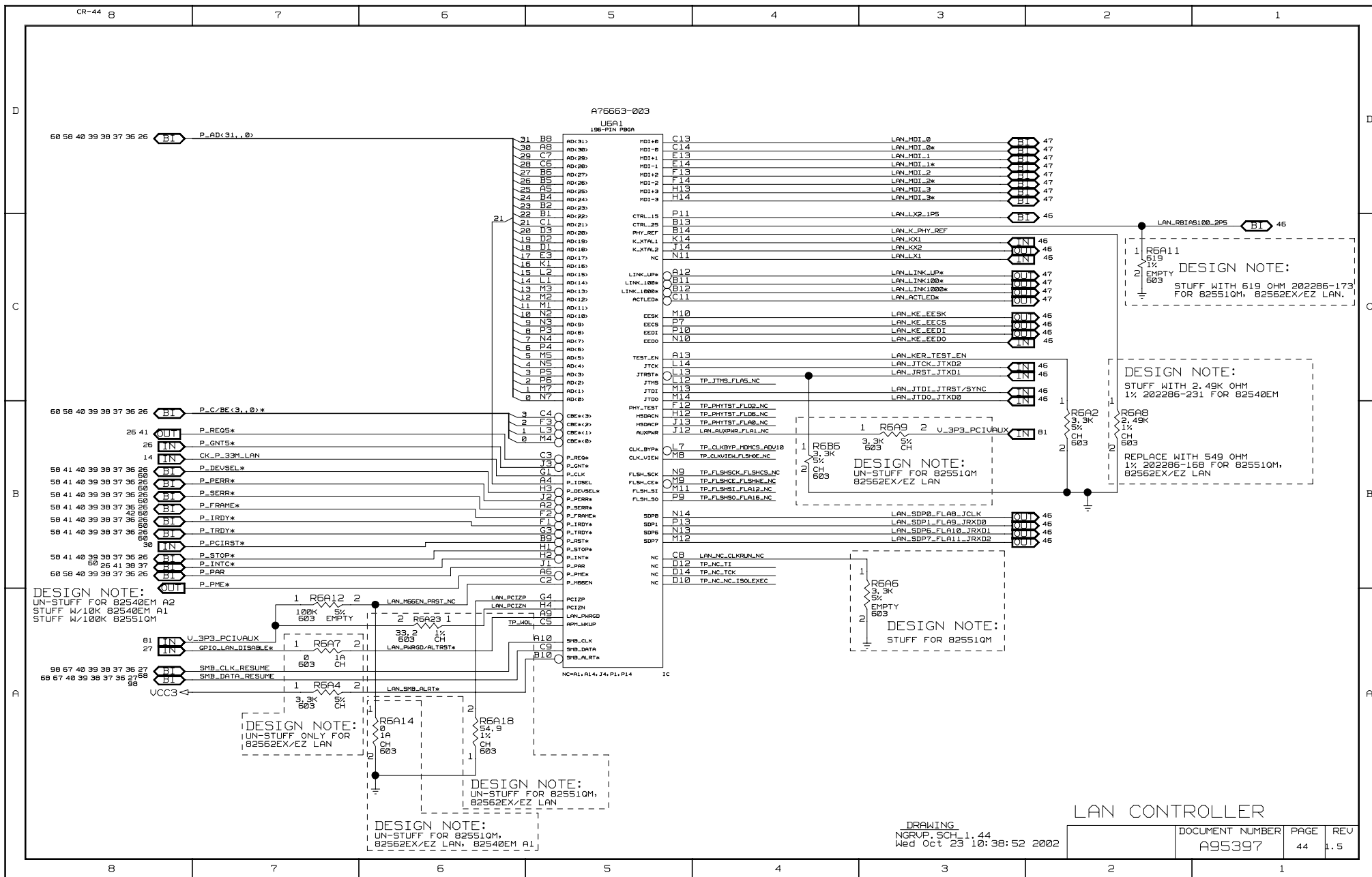


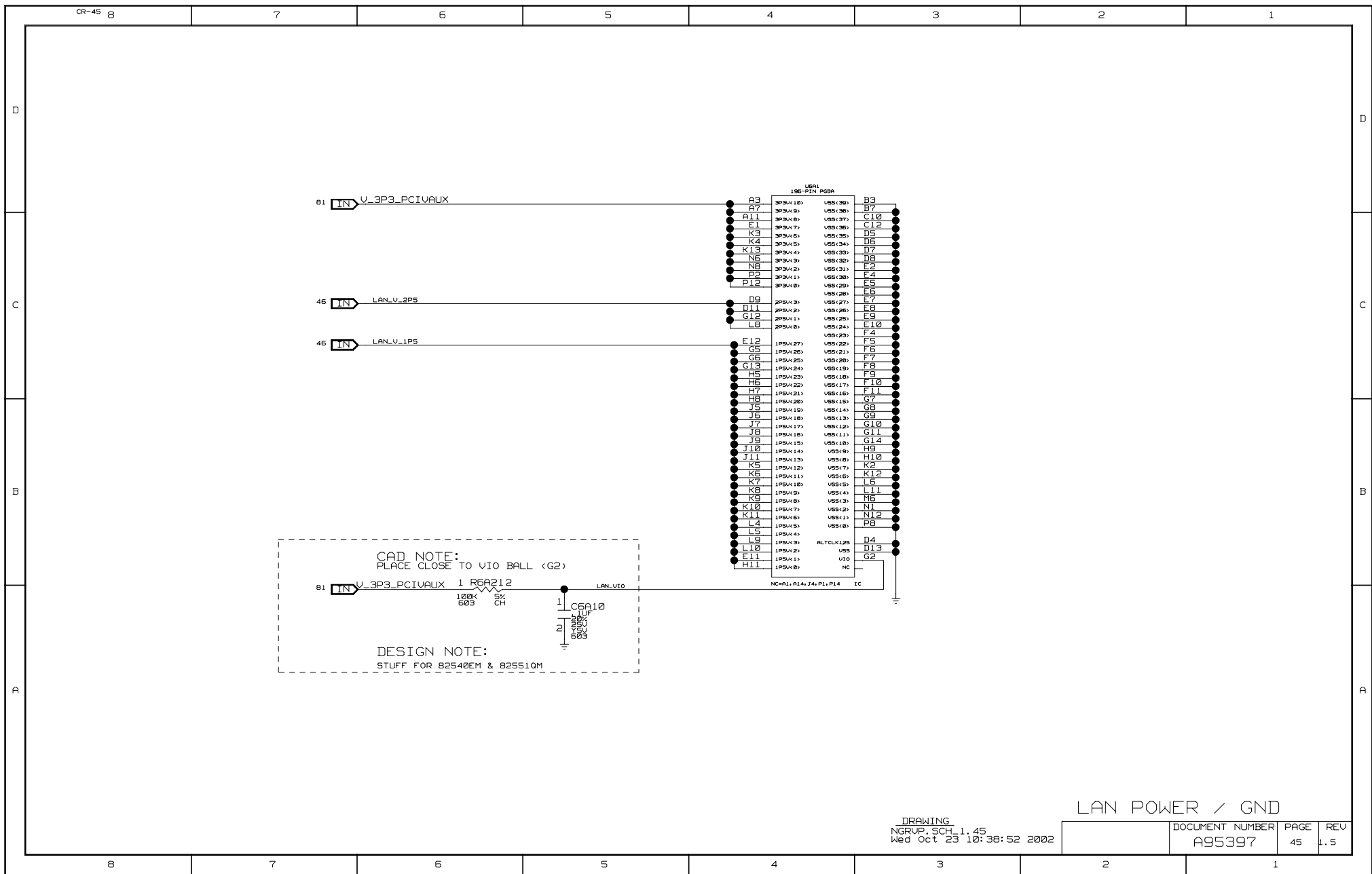


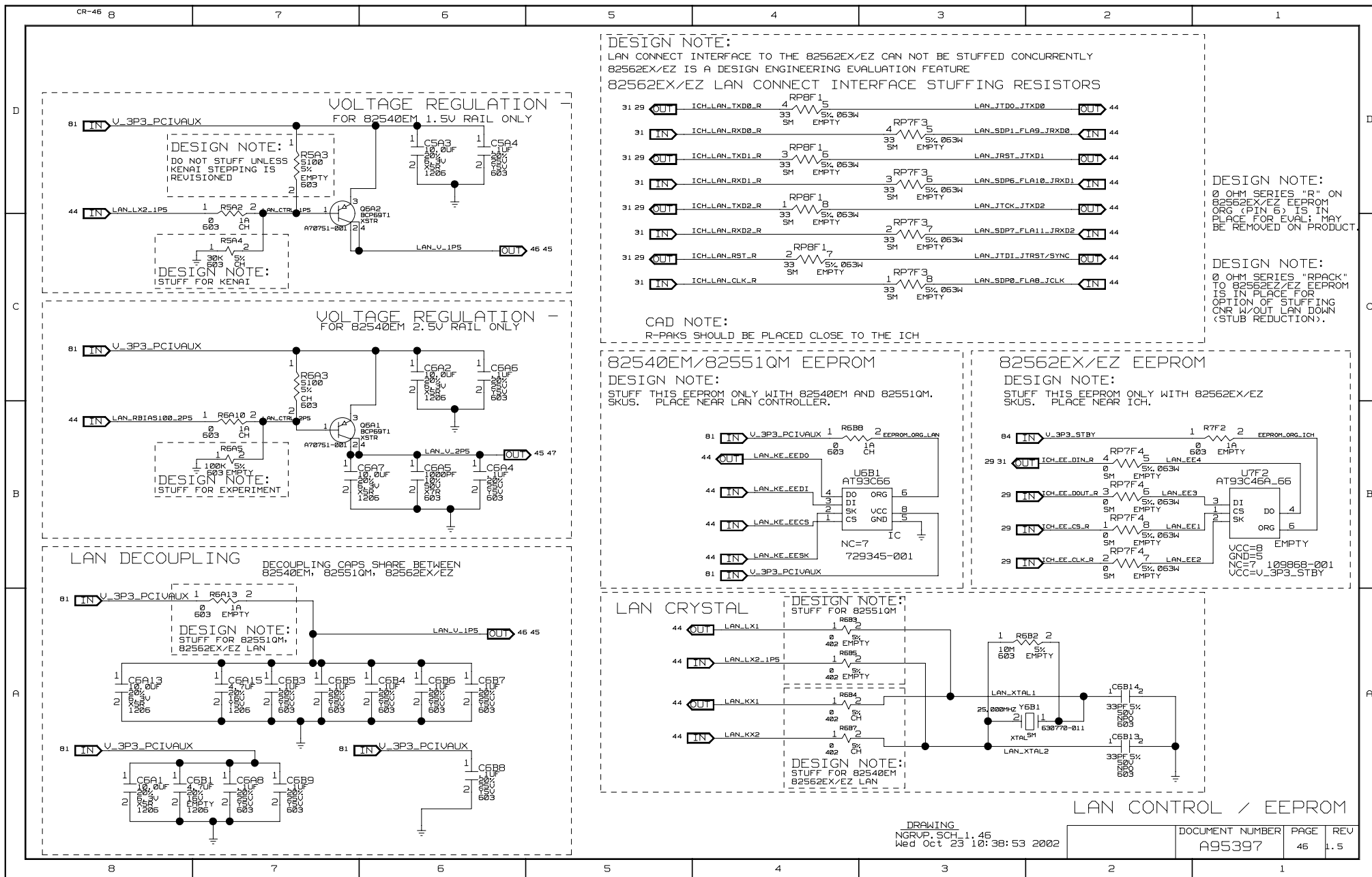


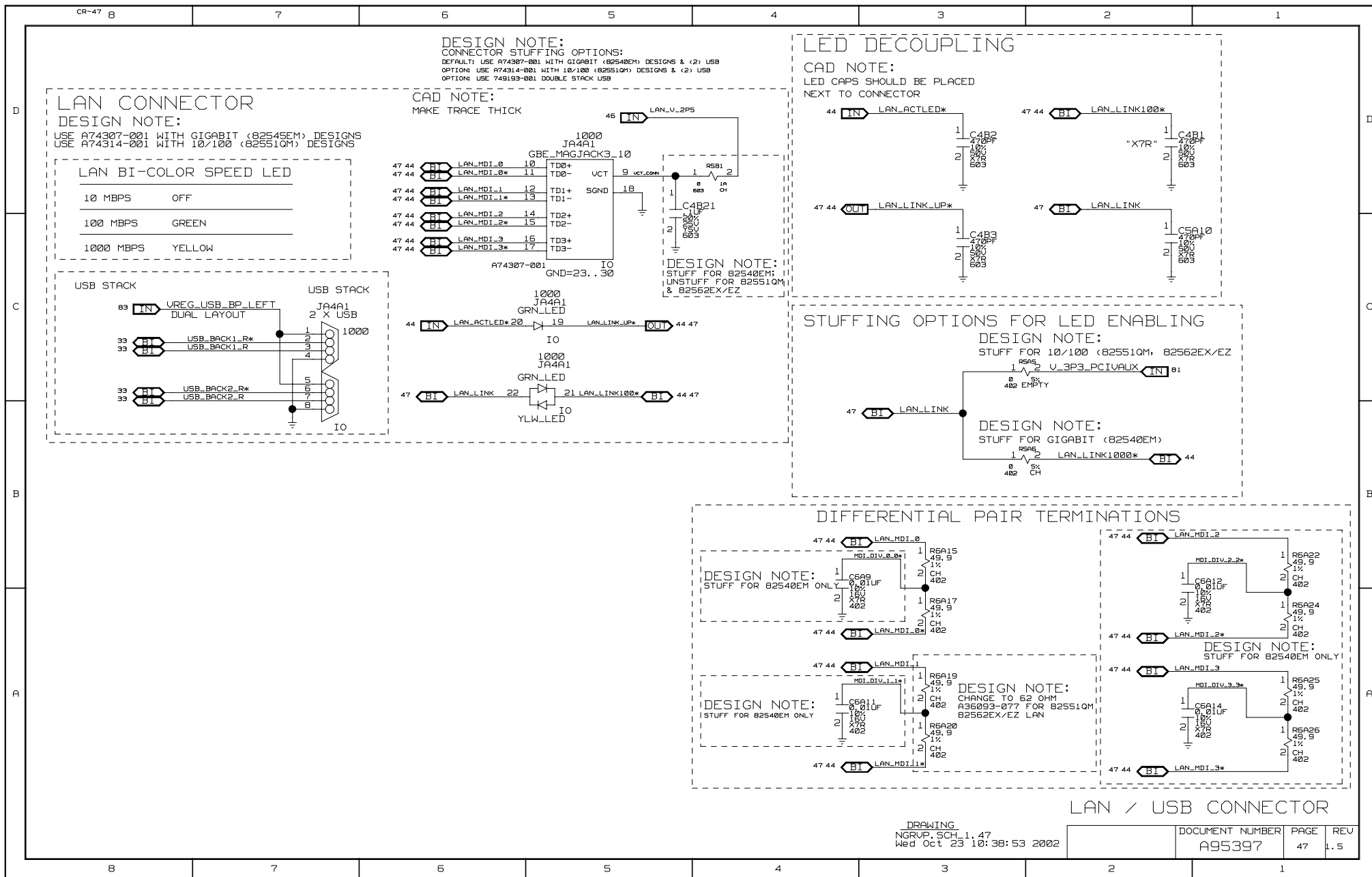


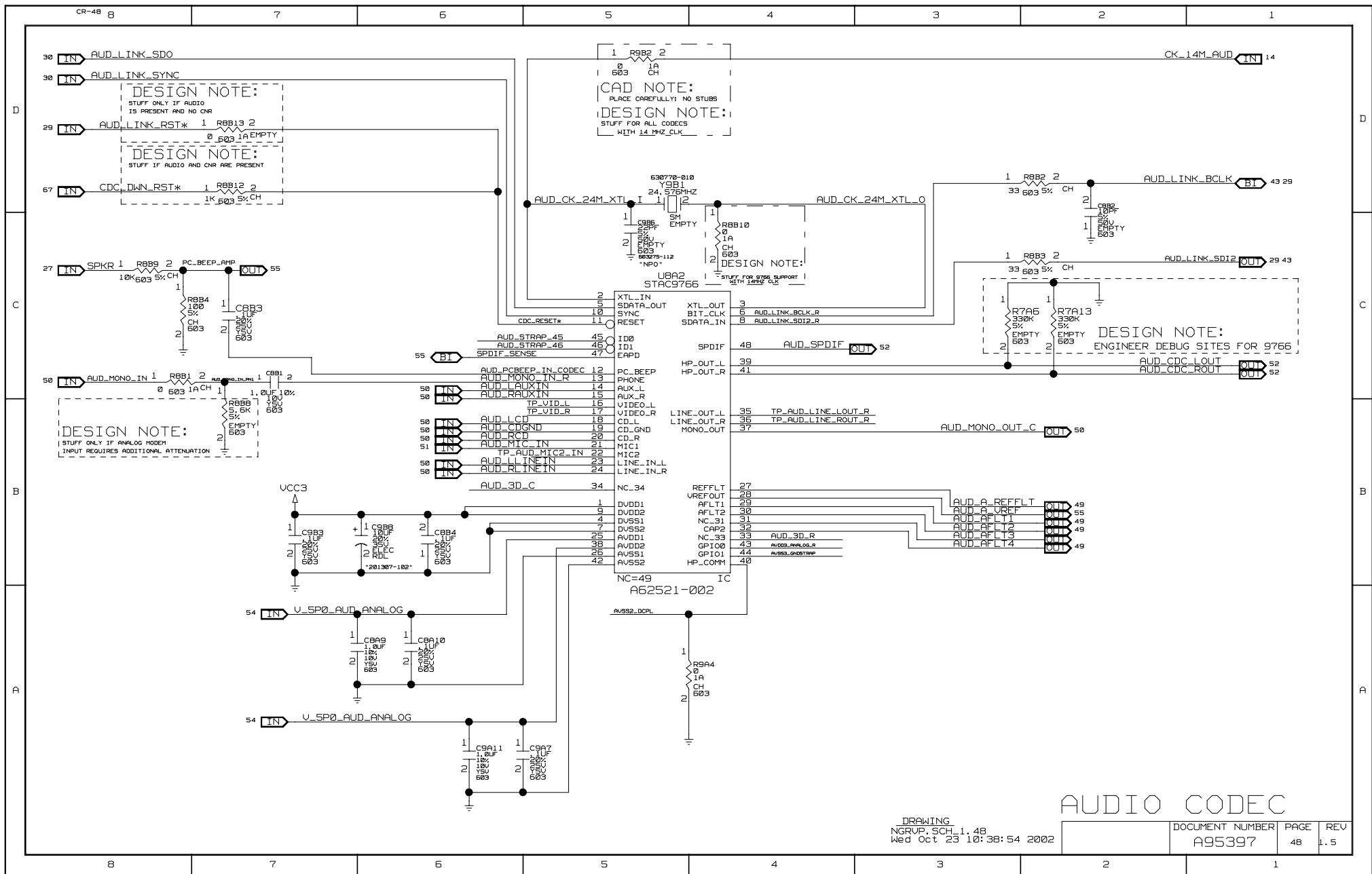


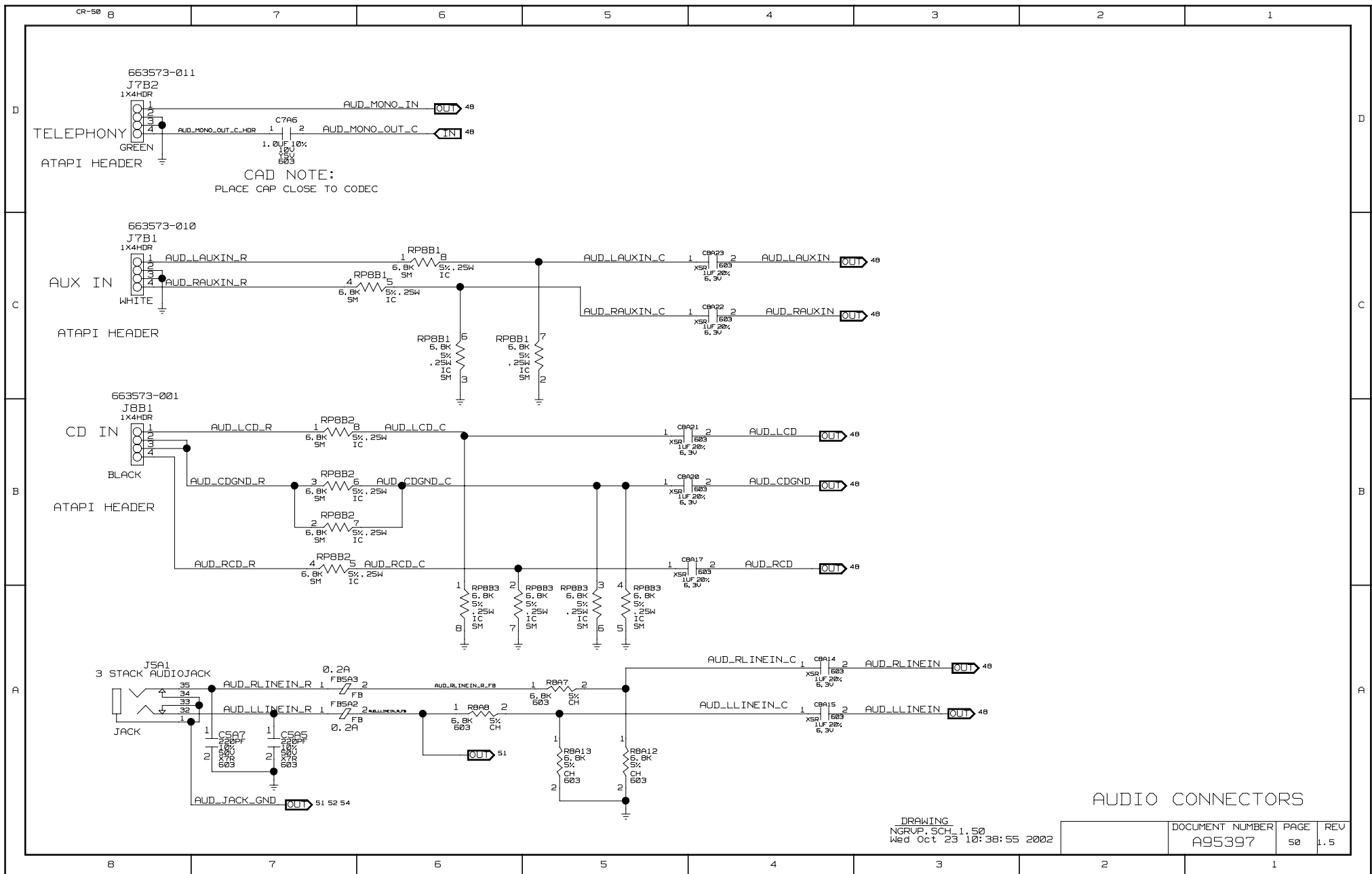








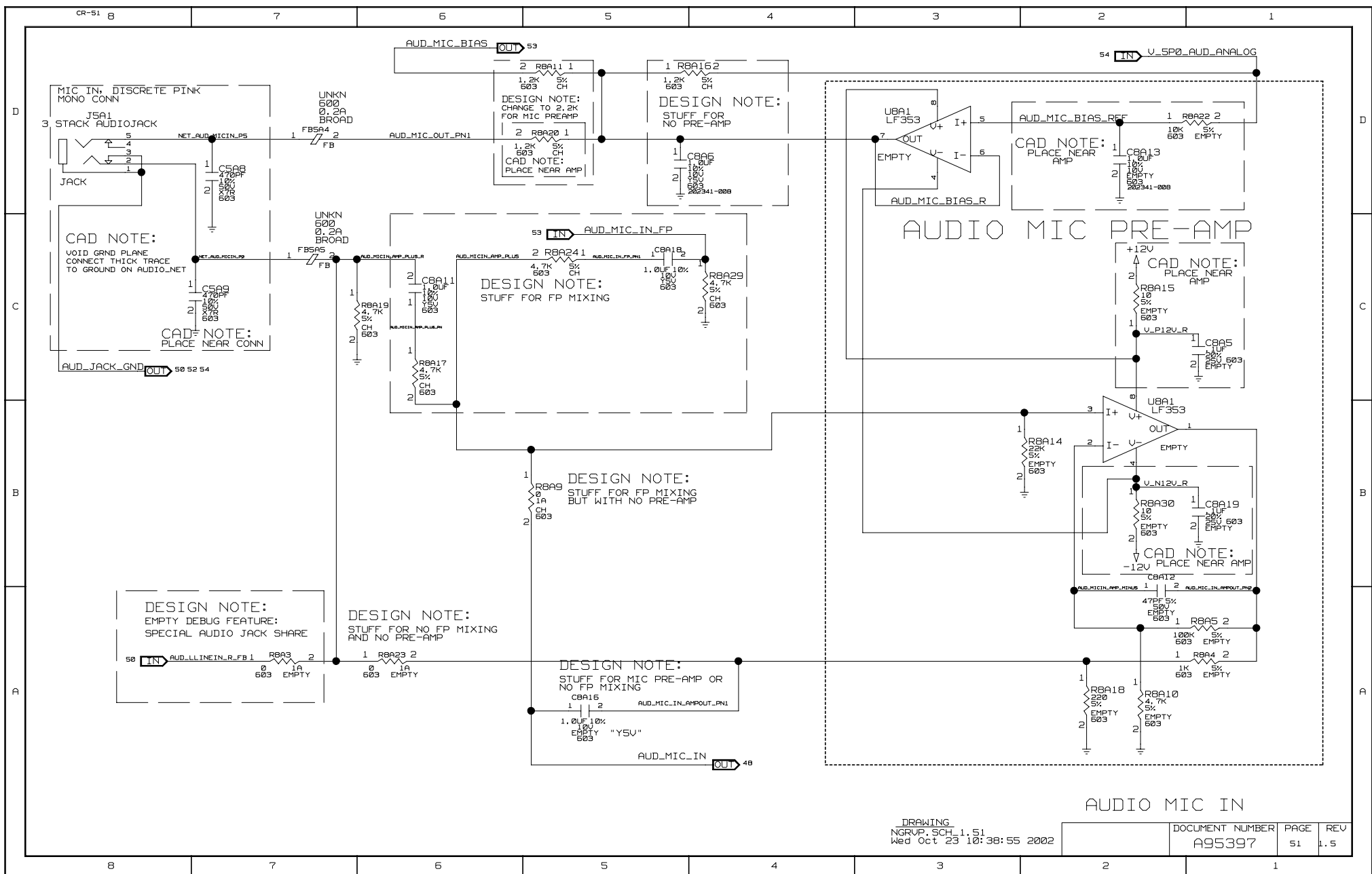


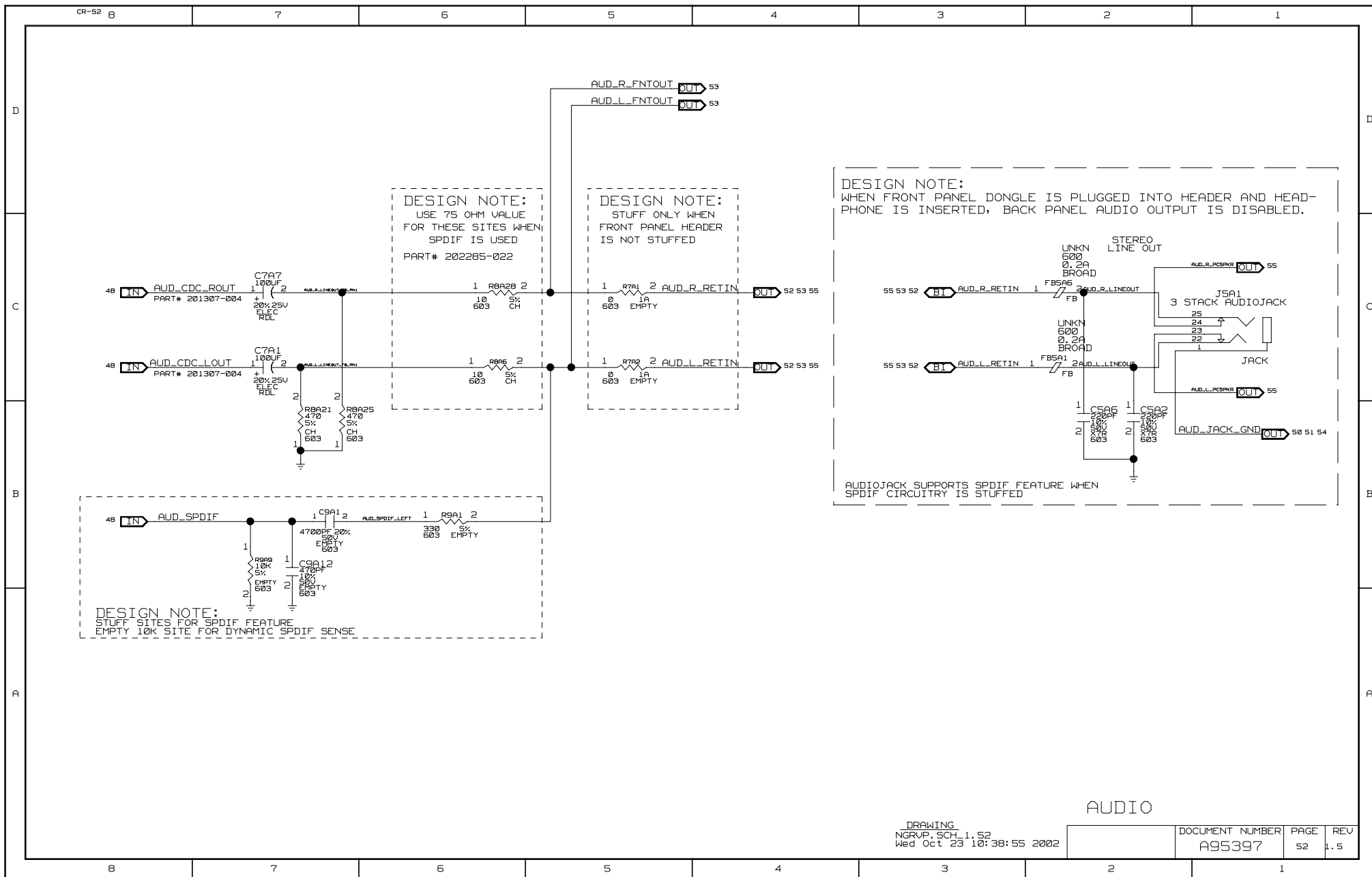


AUDIO CONNECTORS

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 NGRUP.SCH_1.50
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 Wed Oct 23 10:38:55 2002

AUDIO

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A95397	52	1.5

DESIGN EVALUATION USES SUITCASE JUMPERS

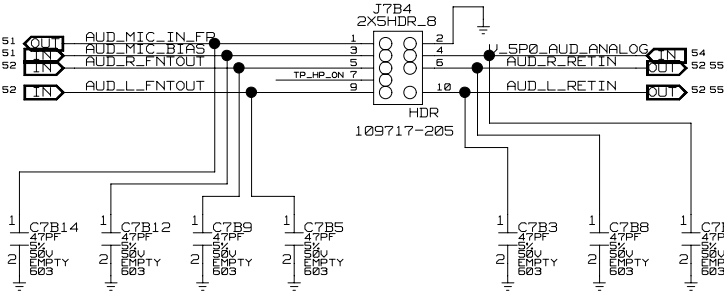
DESIGN NOTE:

FRONT PANEL DONGLE W/OUTPUT PLUG MUST HAVE SPRING CLIPS ROUTED BACK TO PINS 6 & 10 TO ALLOW BACK PANEL AUDIO AS ALTERNATIVE WHEN HP-JACK ISN'T PLUGGED INTO FRONT PANEL

DESIGN NOTE:

WHEN NO FRONT PANEL DONGLE IS PLUGGED INTO HEADER, SUITCASE JUMPERS CAN BE PLACED ON PIN 5-6, 9-10 TO ALLOW BACK PANEL AUDIO OUTPUT

DEFAULT CONFIGURATION IS FOR FP DONGLE



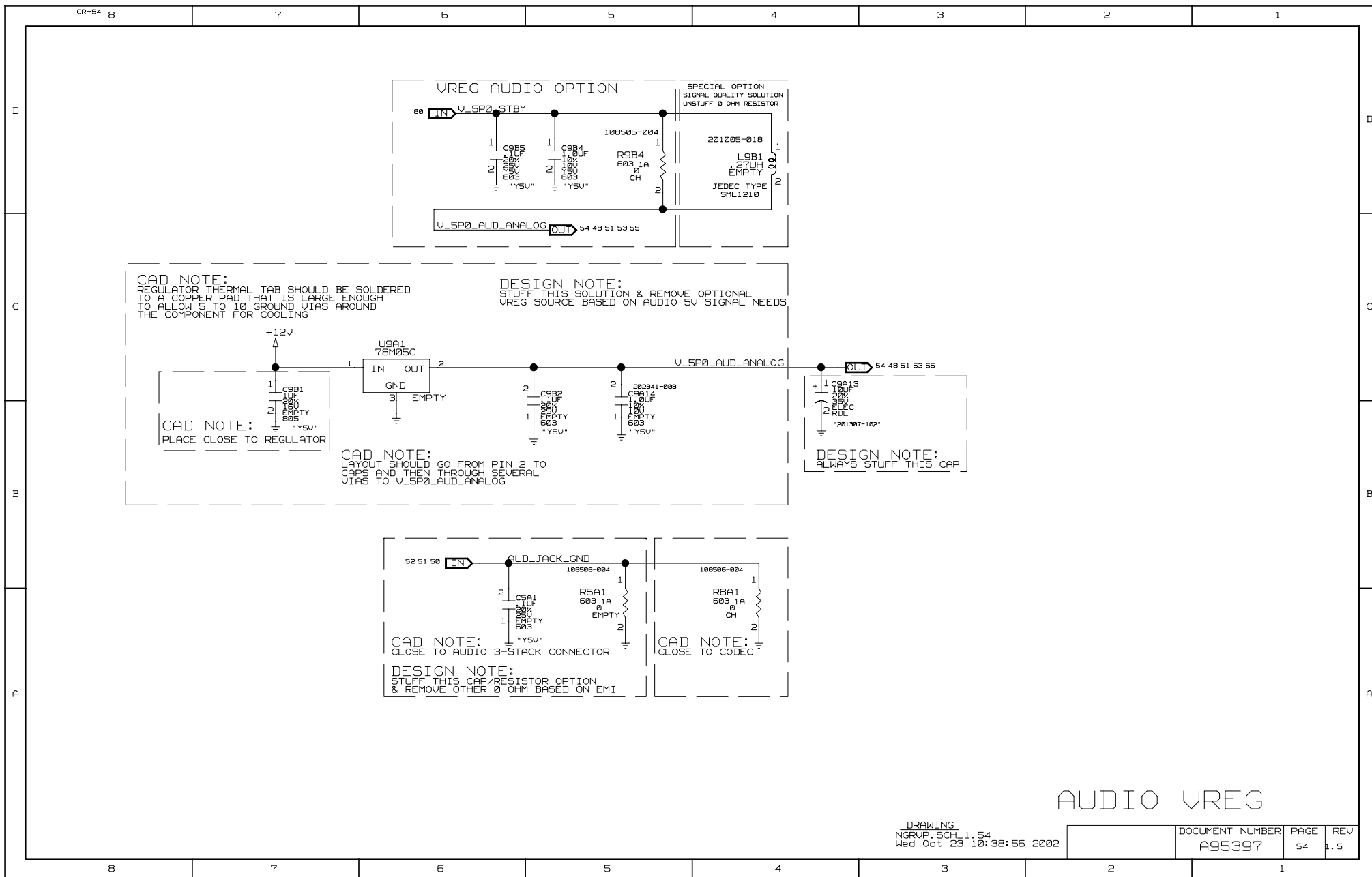
CAD NOTE:

PLACE NEAR AUDIO CIRCUIT

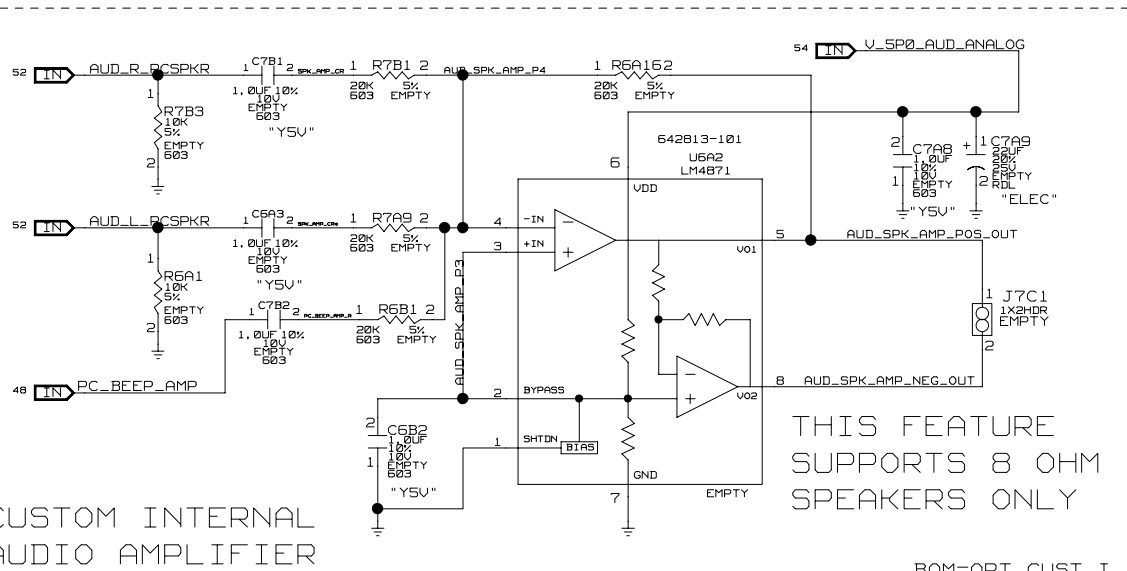
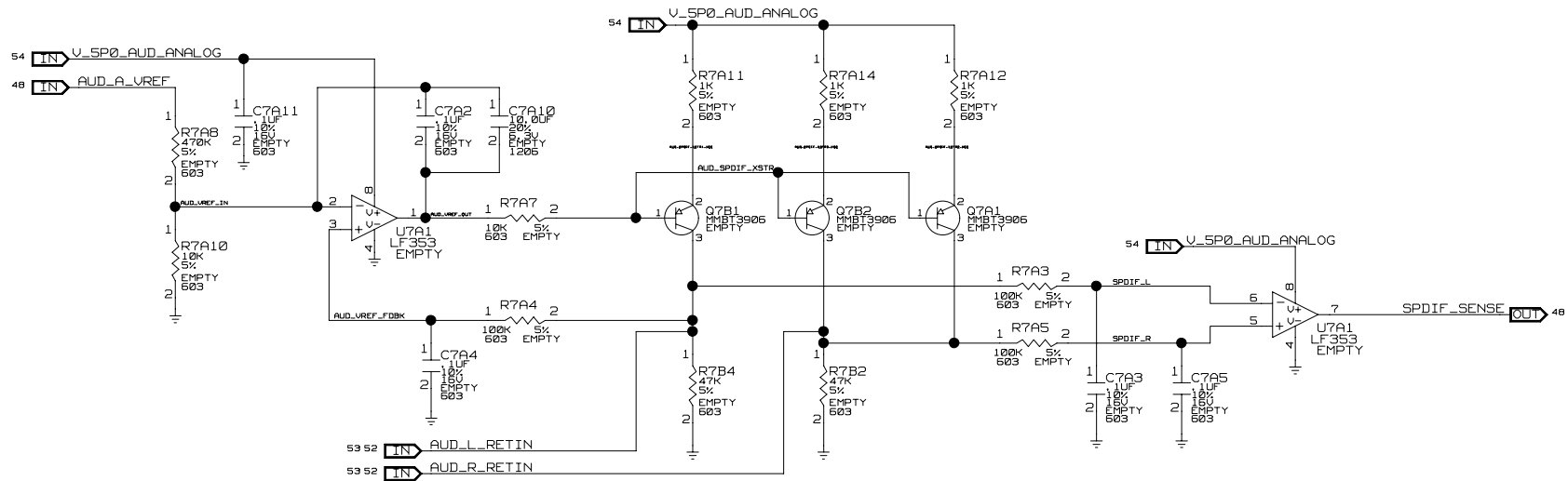
AUDIO FRONT PANEL

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NGRUP.SCH_1.53
Wed Oct 23 10:38:56 2002

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FOR AUDIO MODULE EVALUATION ONLY; SPDIF SENSE SUPPORT;



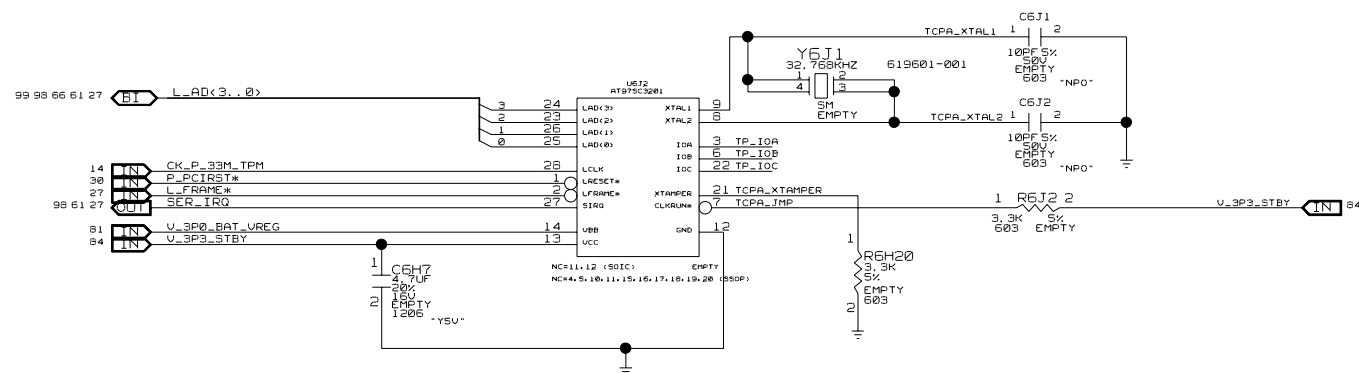
THIS FEATURE SUPPORTS 8 OHM SPEAKERS ONLY

SP DIF / CUSTOM FEATURE

DRAWING	DOCUMENT NUMBER	PAGE	REV
NGRUP_SCH_1.55	A95397	55	1.5
Wed Oct 23 10:38:56 2002			

BOM=OPT_CUST_I

SECURITY: TPM (TRUSTED PLATFORM MODULE)

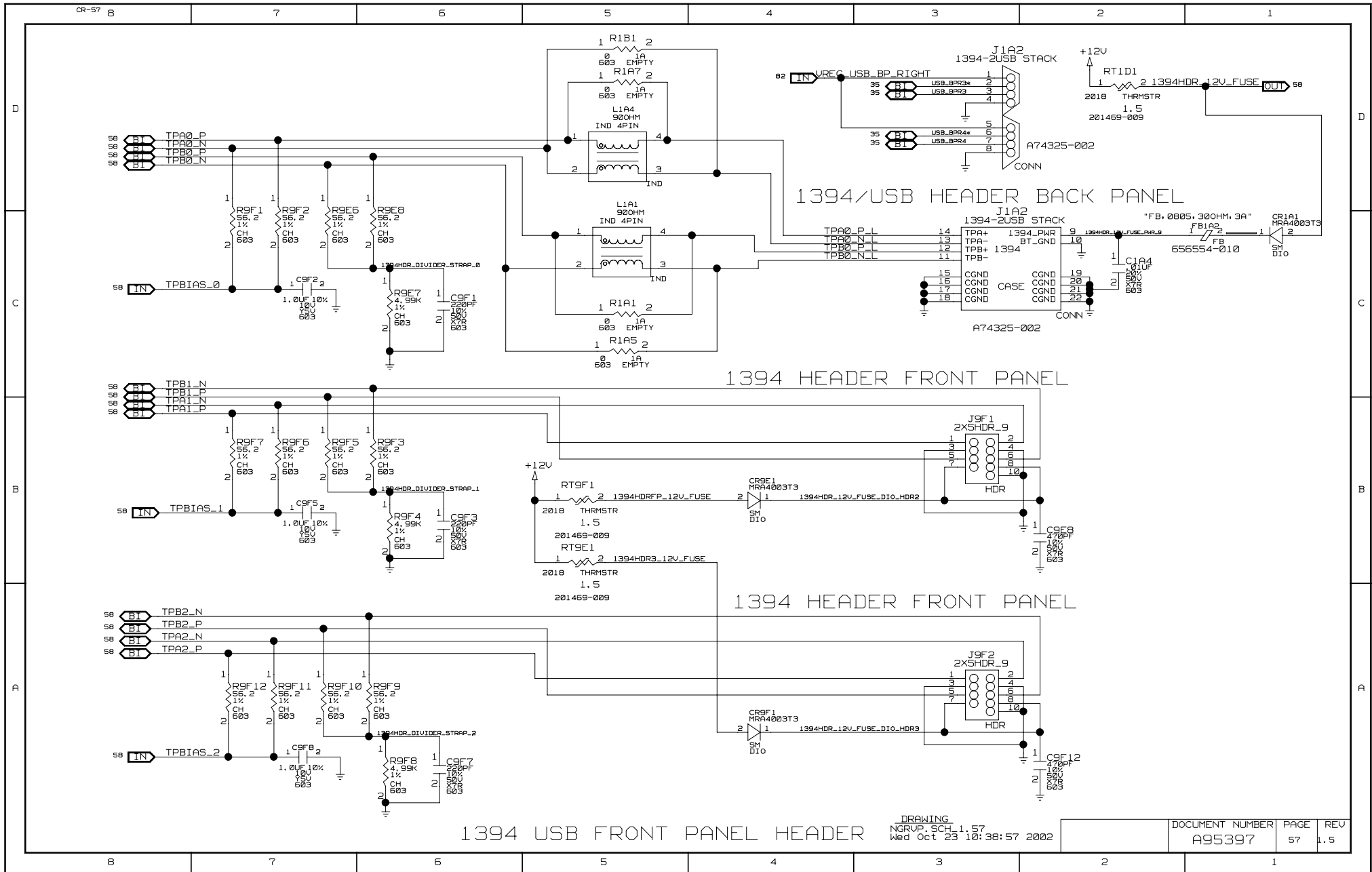


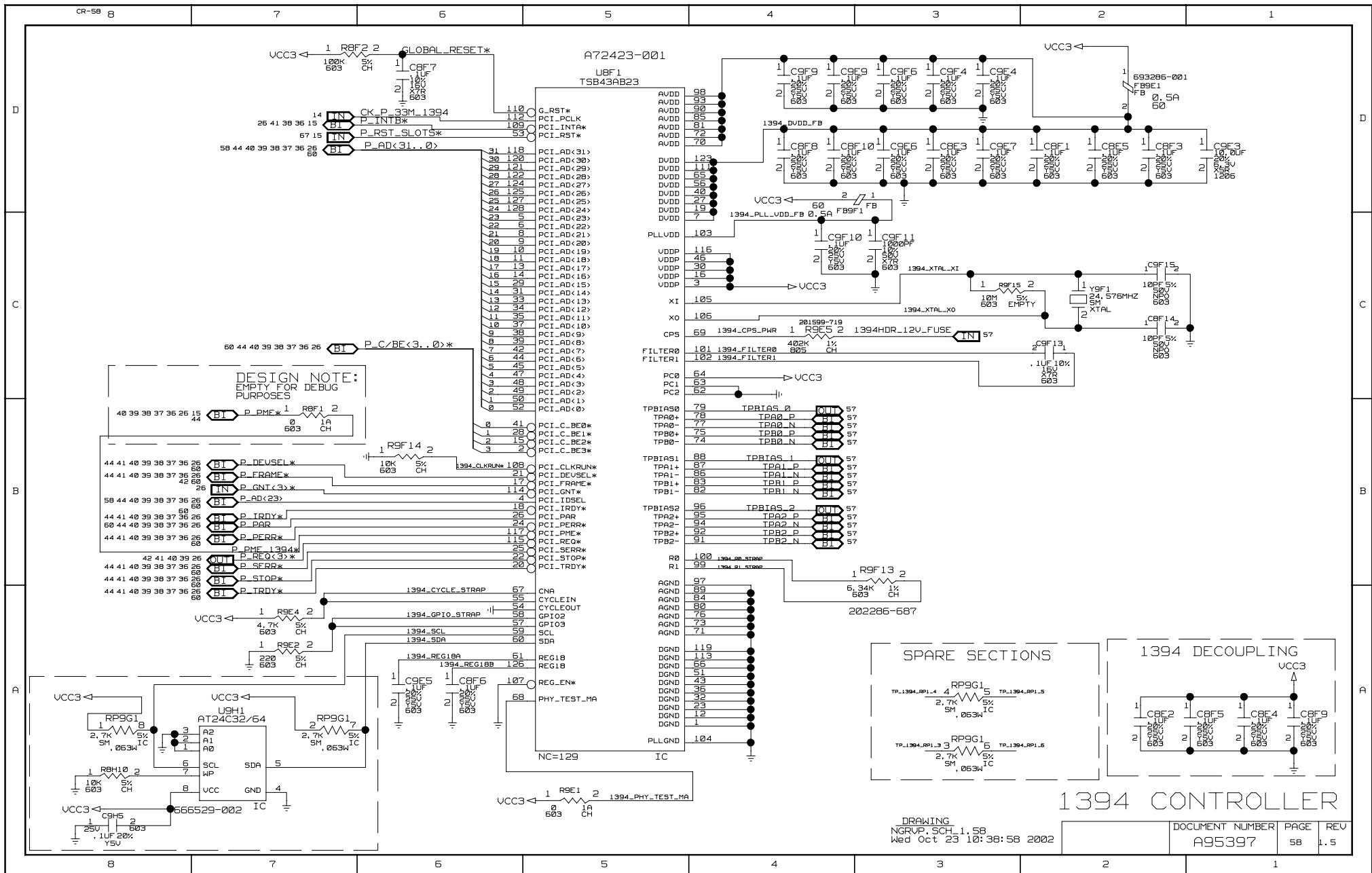
ATMEL AT97SC3201

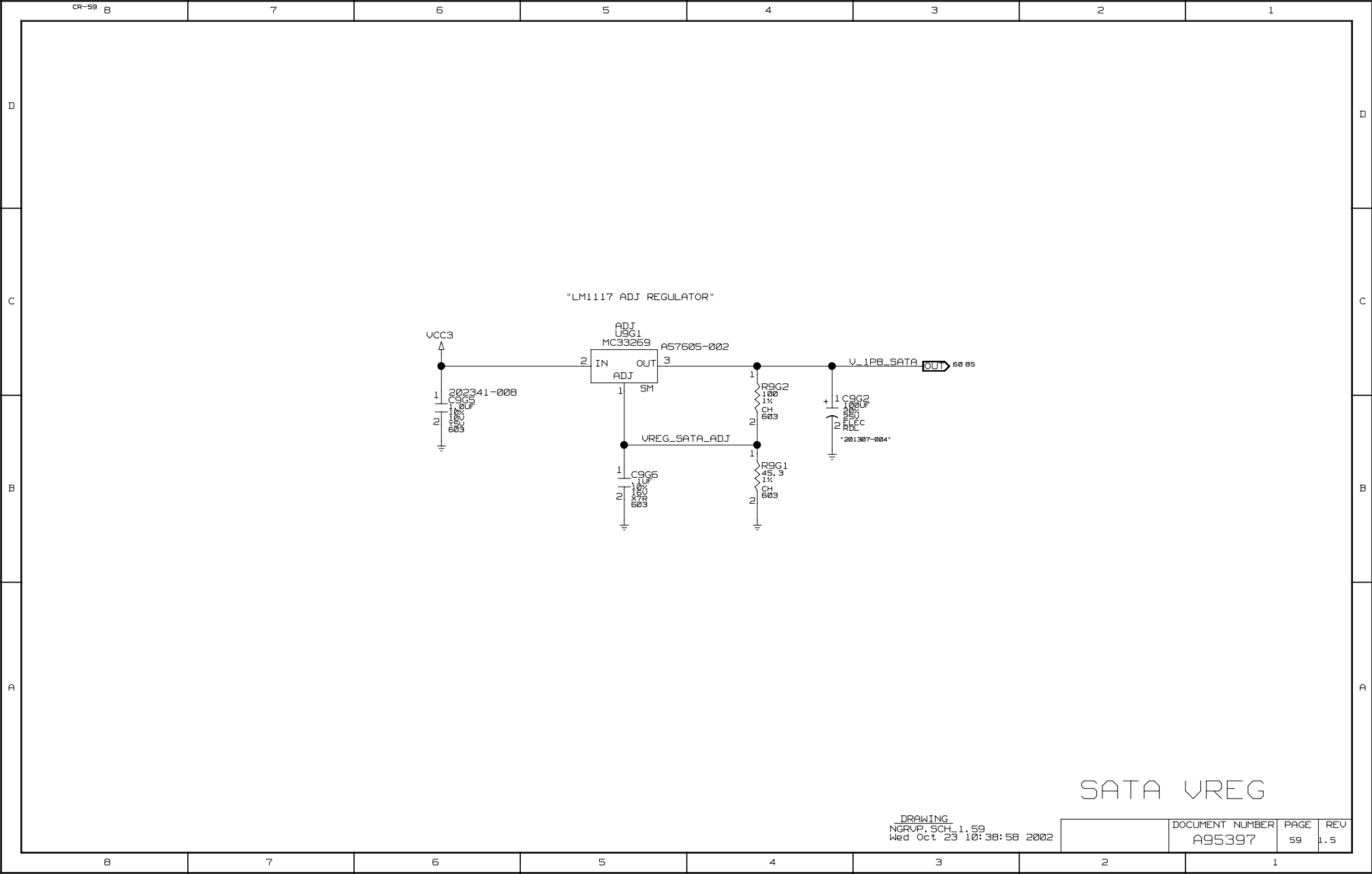
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Wed Oct 23 10:38:57 2002

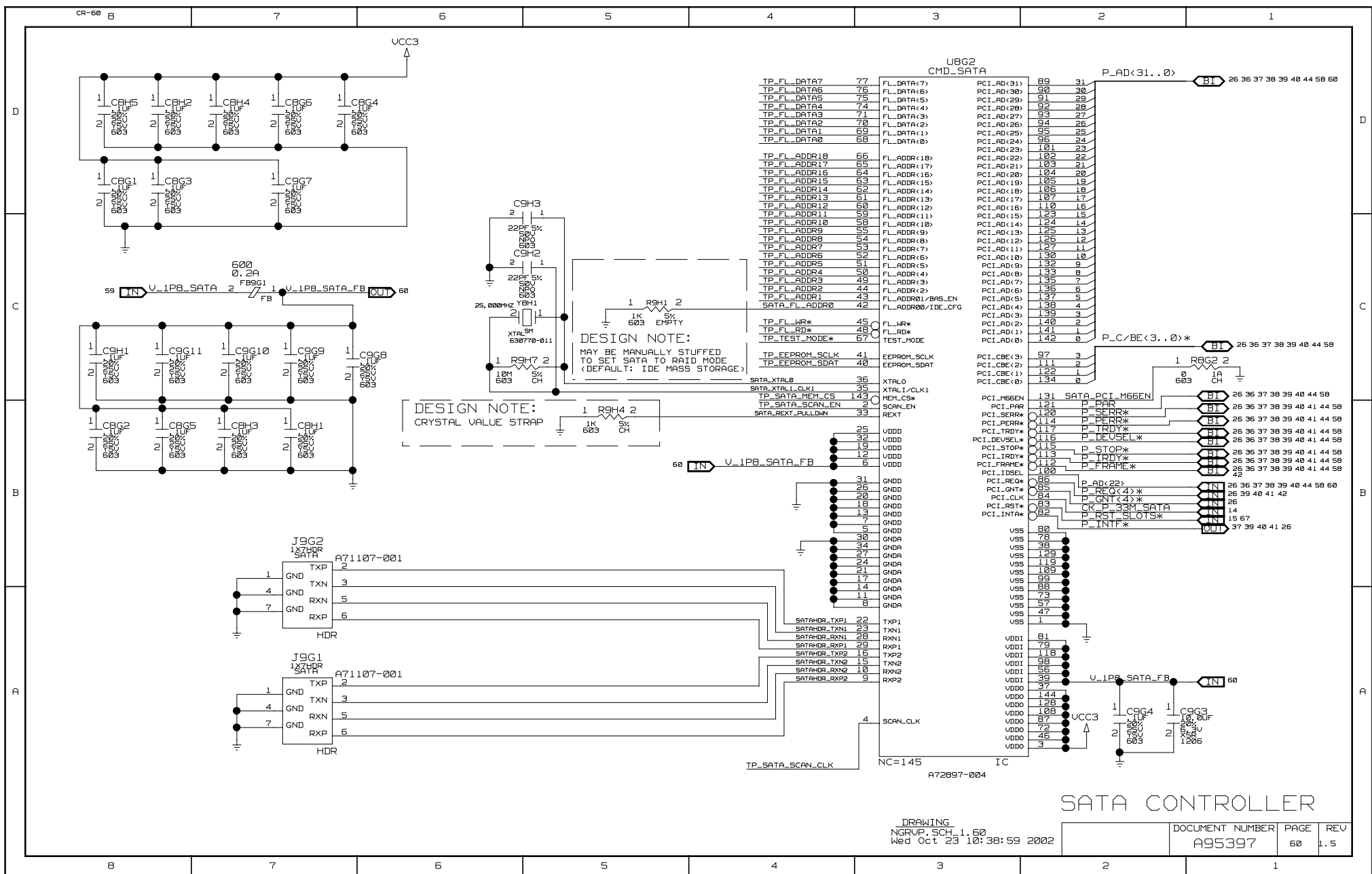
TRUSTED PLATFORM MODULE

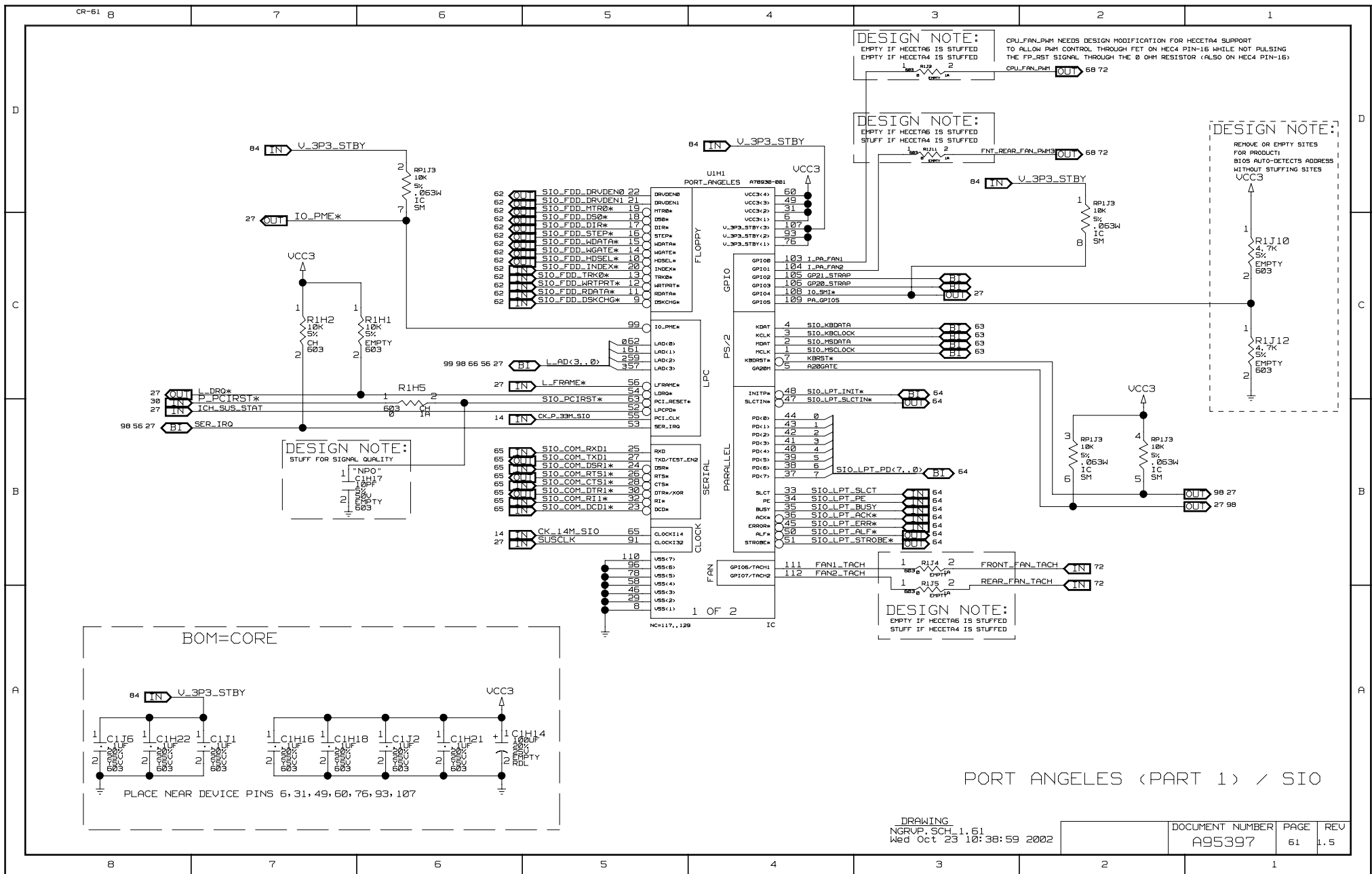
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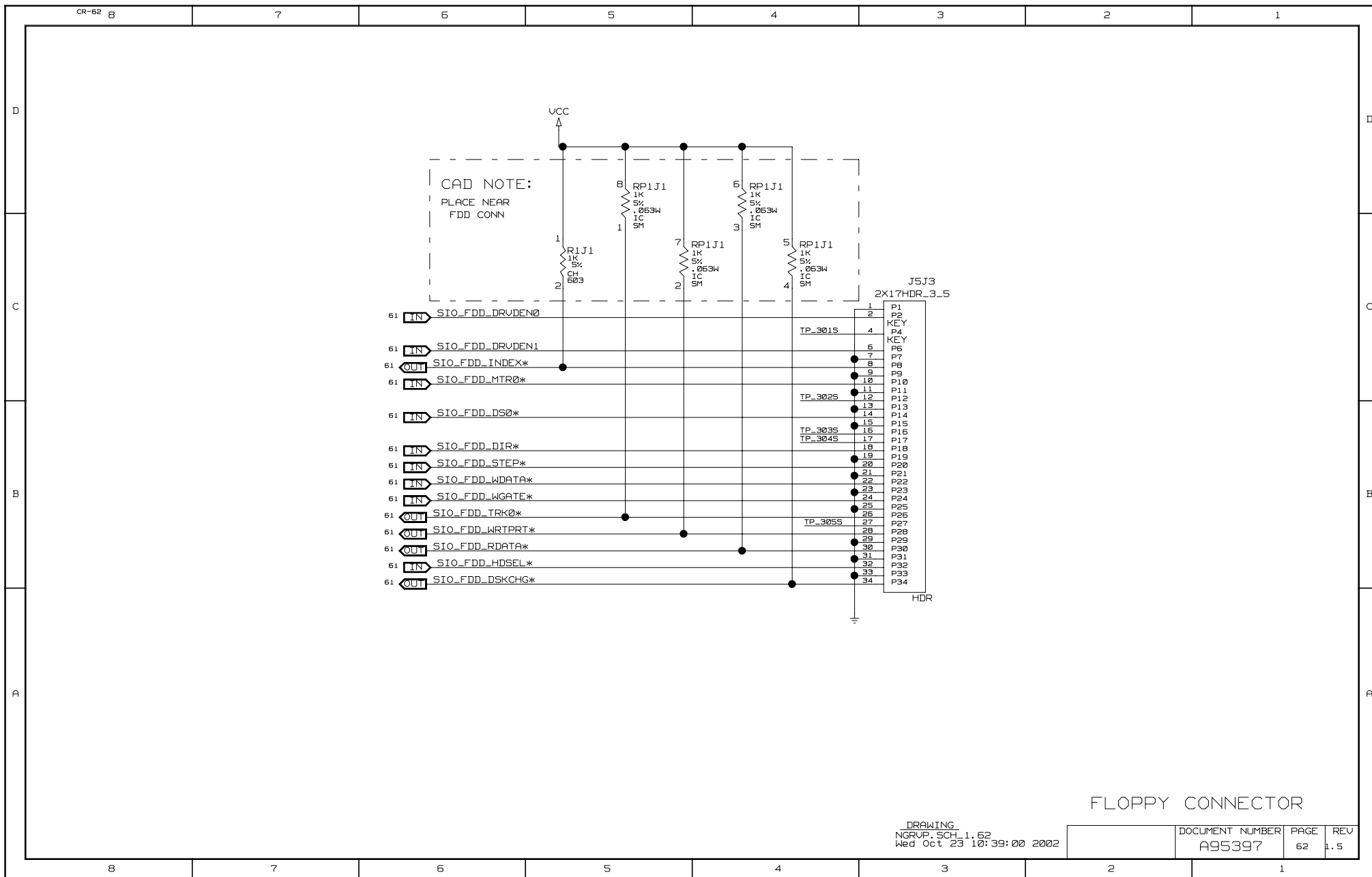








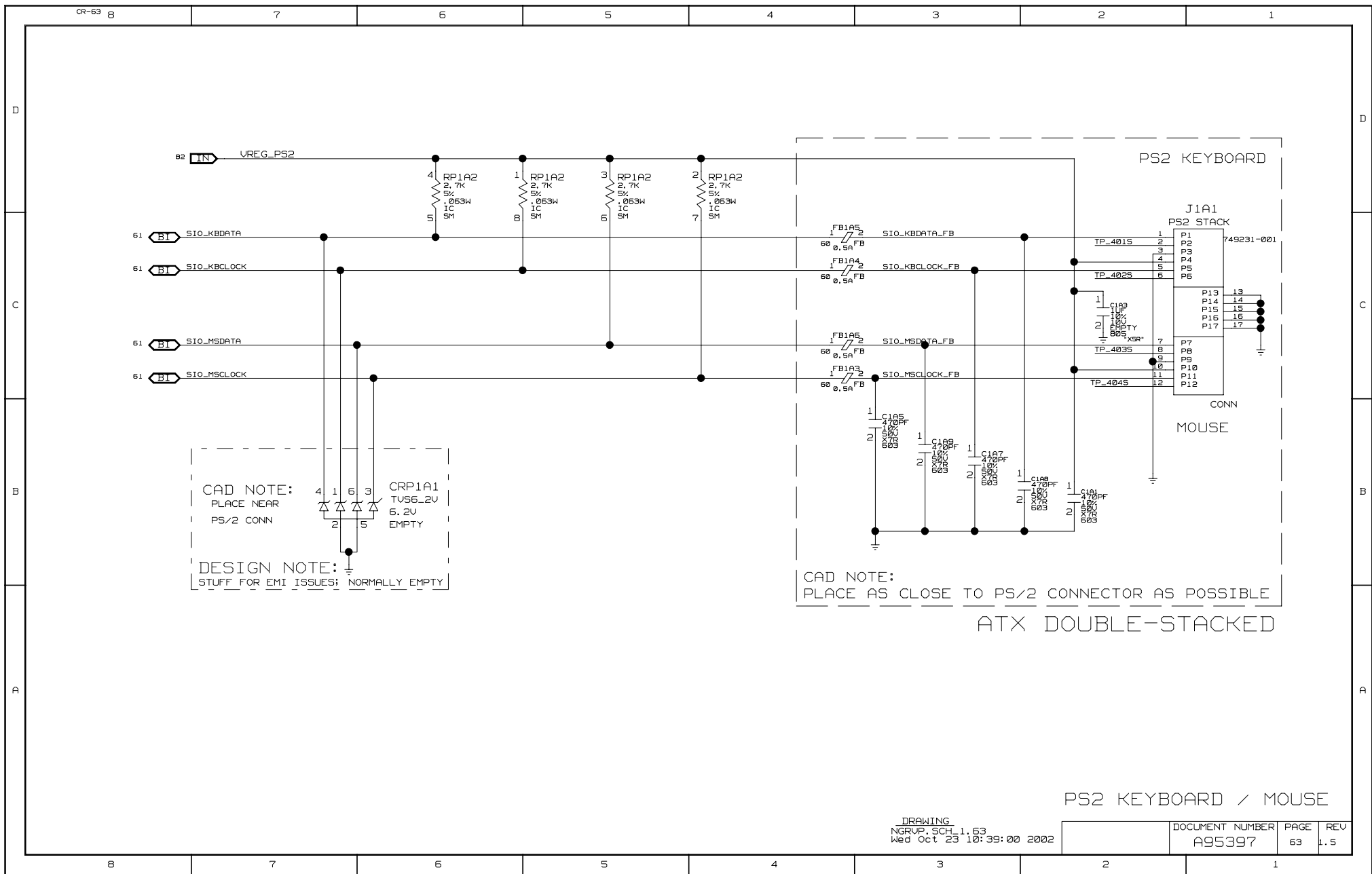


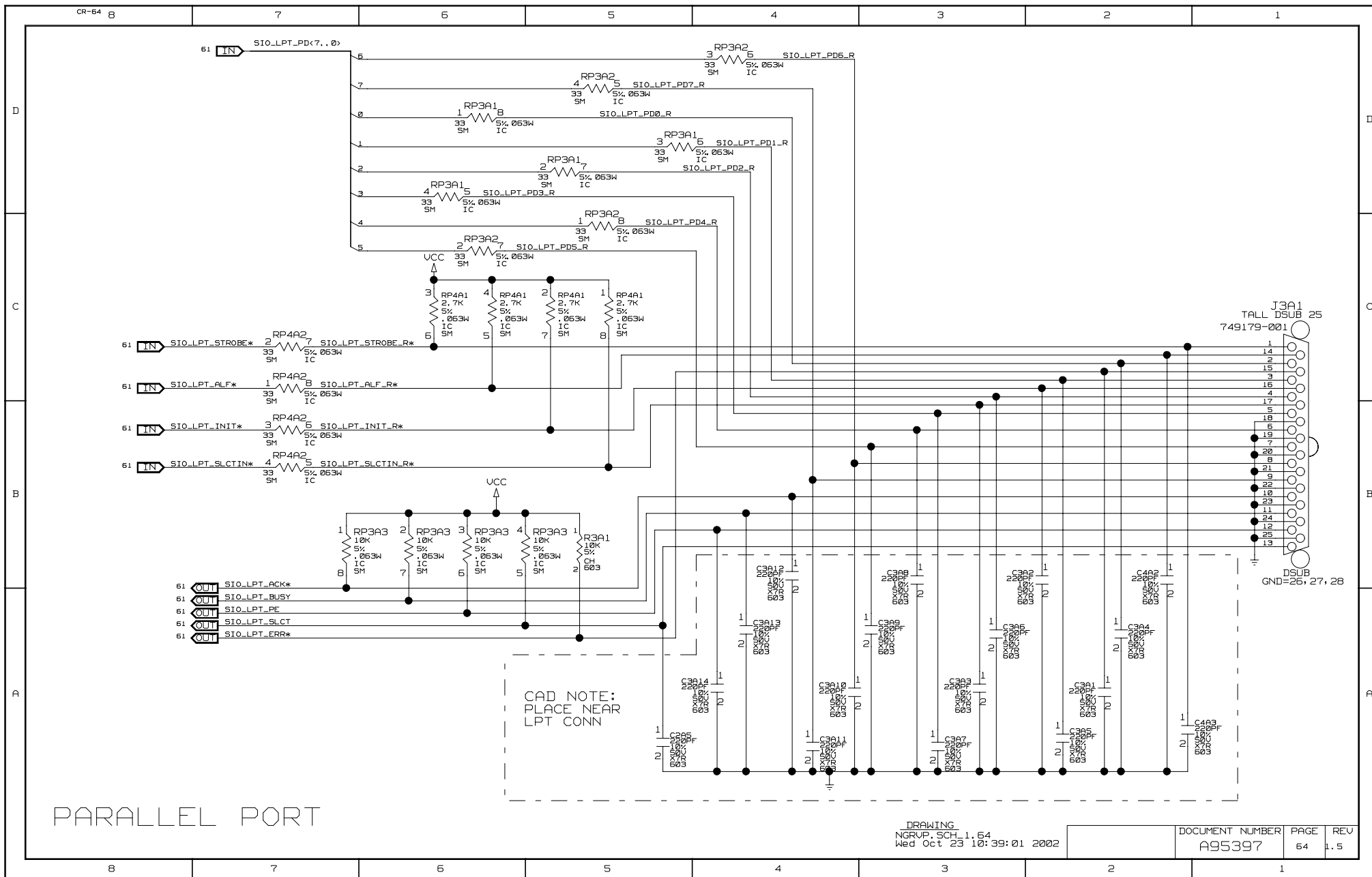


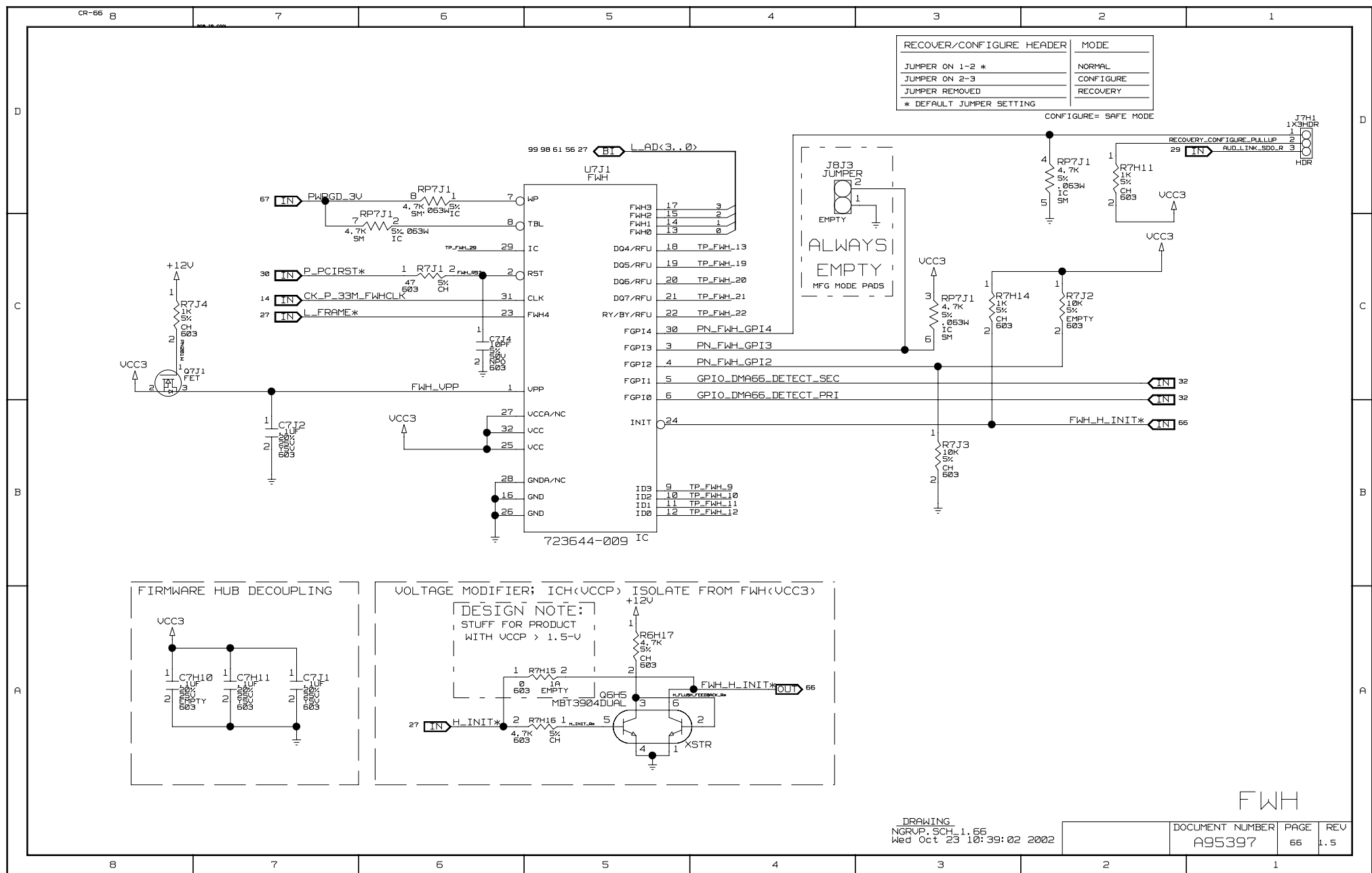
FLOPPY CONNECTOR

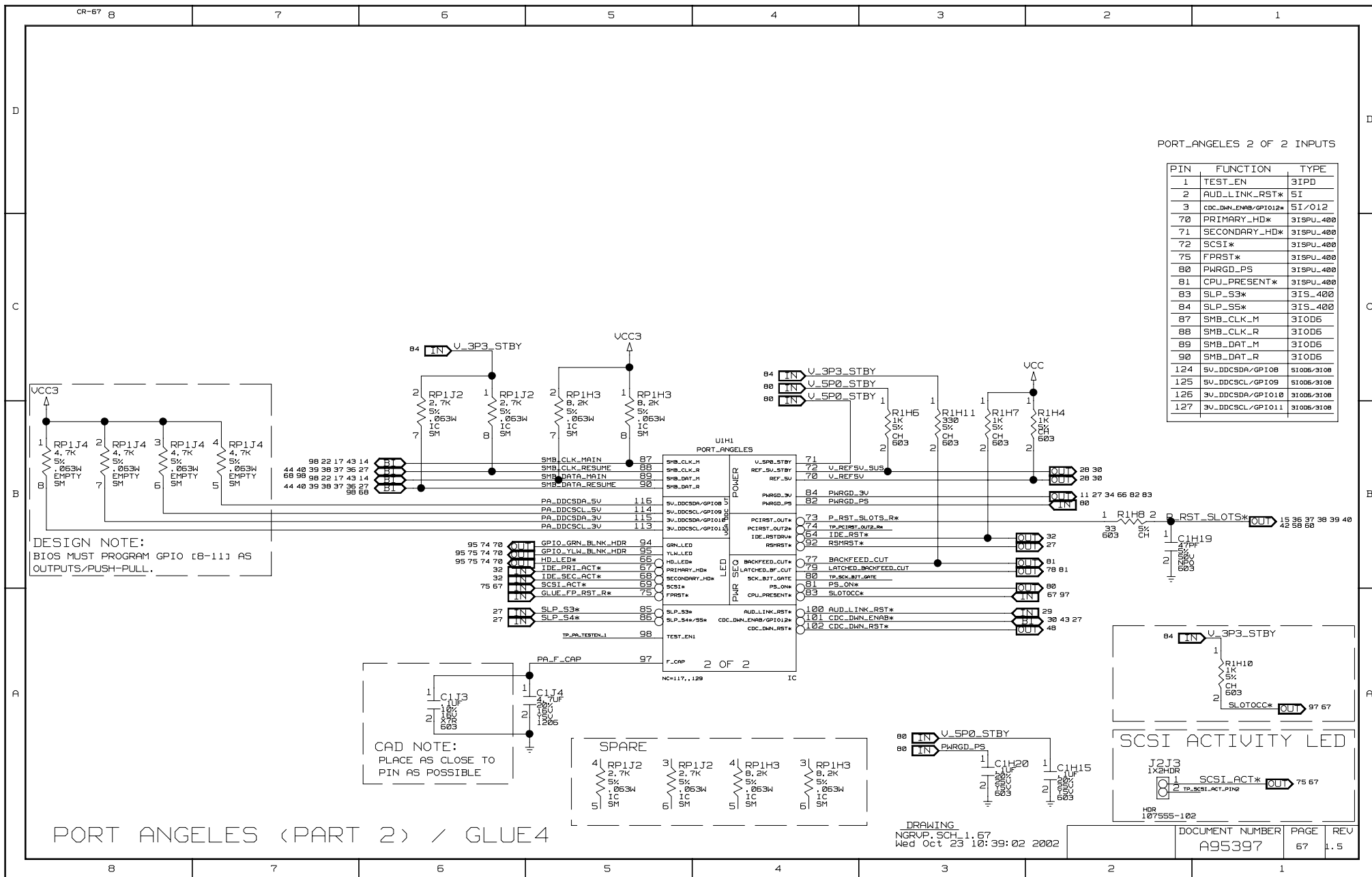
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Wed Oct 23 10:39:00 2002

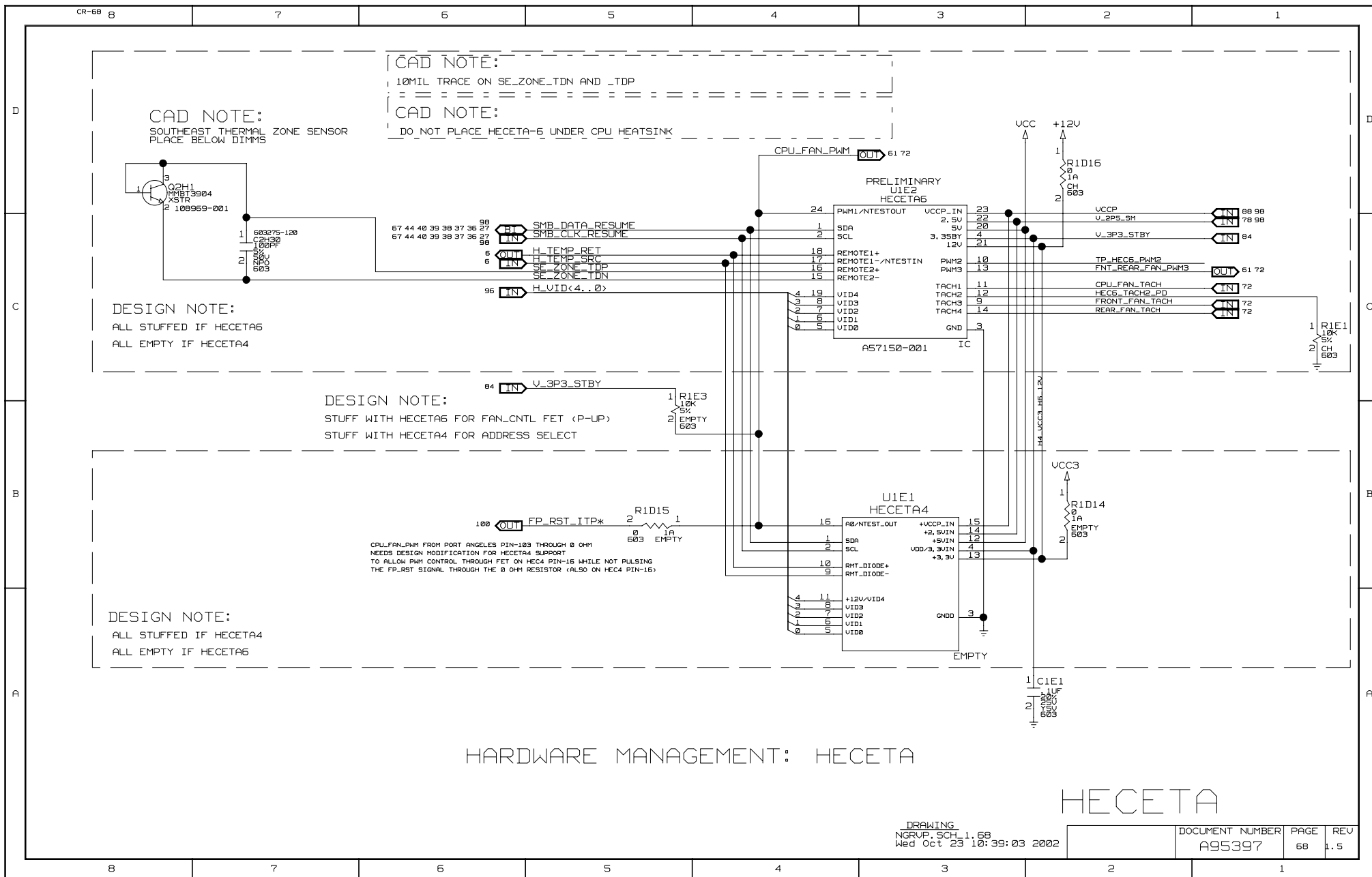
DOCUMENT NUMBER	PAGE	REV
A95397	62	1.5







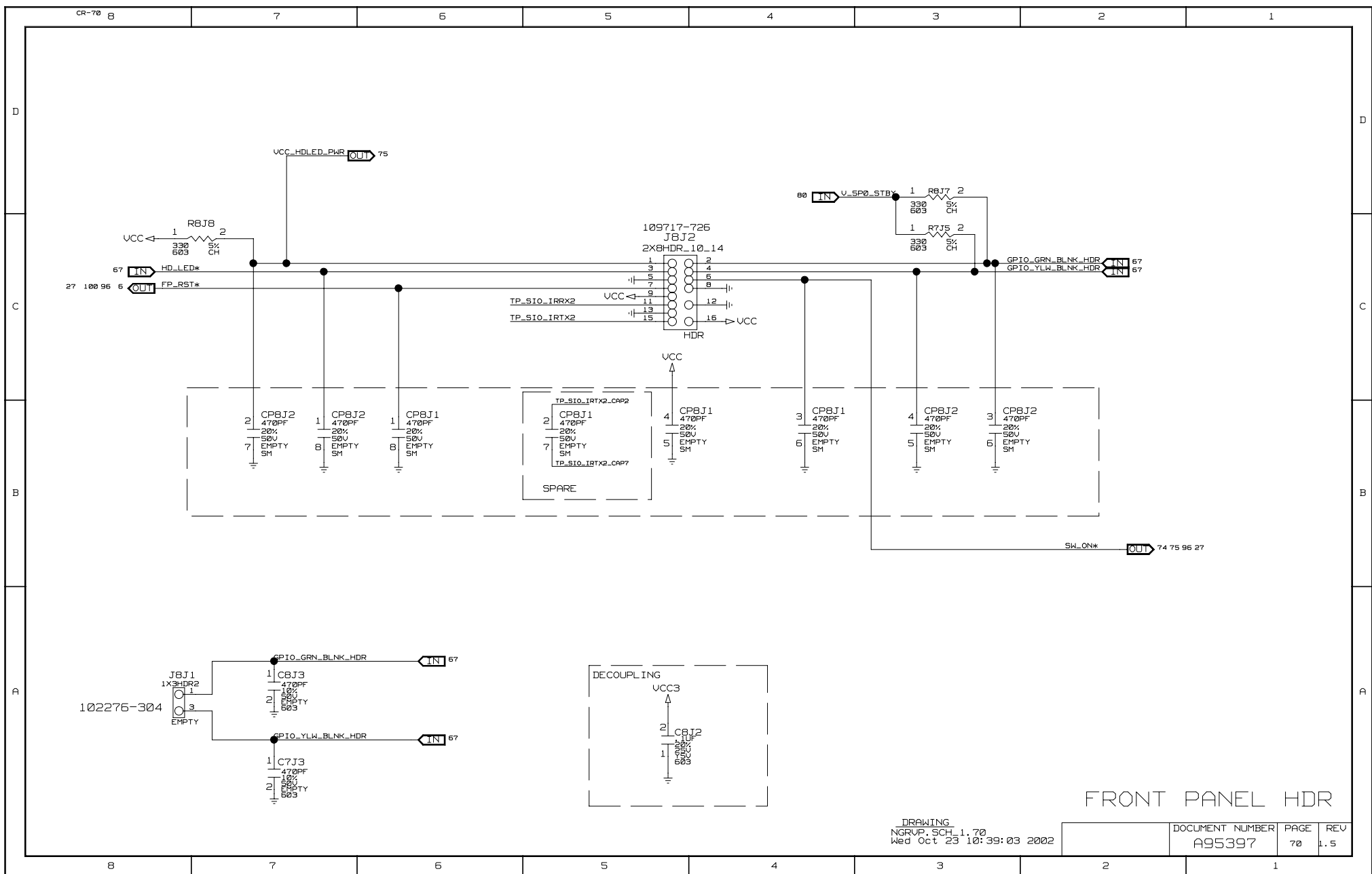


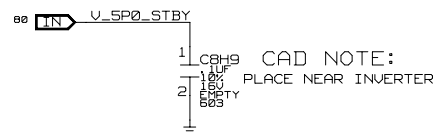
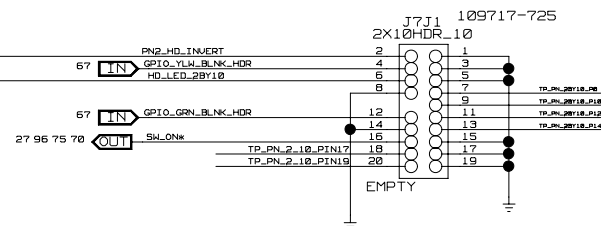




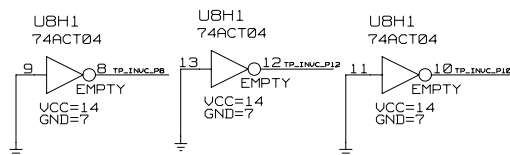
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NGRVP, SCH_1.69
Wed Oct 23 10:39:03 2002

DOCUMENT NUMBER	PAGE	REV
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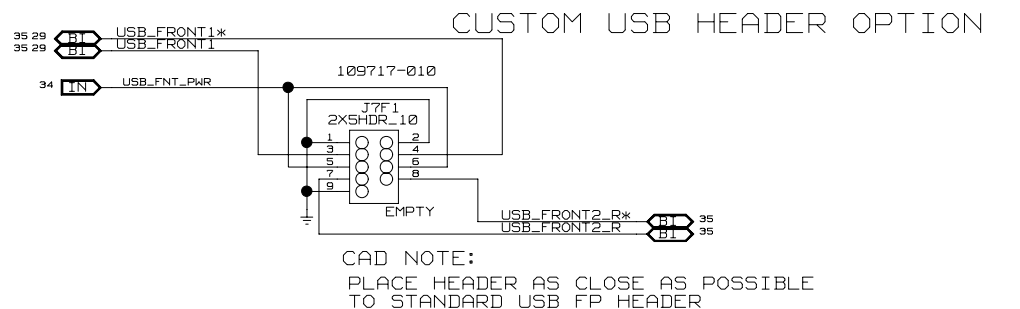




```
VCC=V_5P0_STBY(~EMAILINVRT)
```



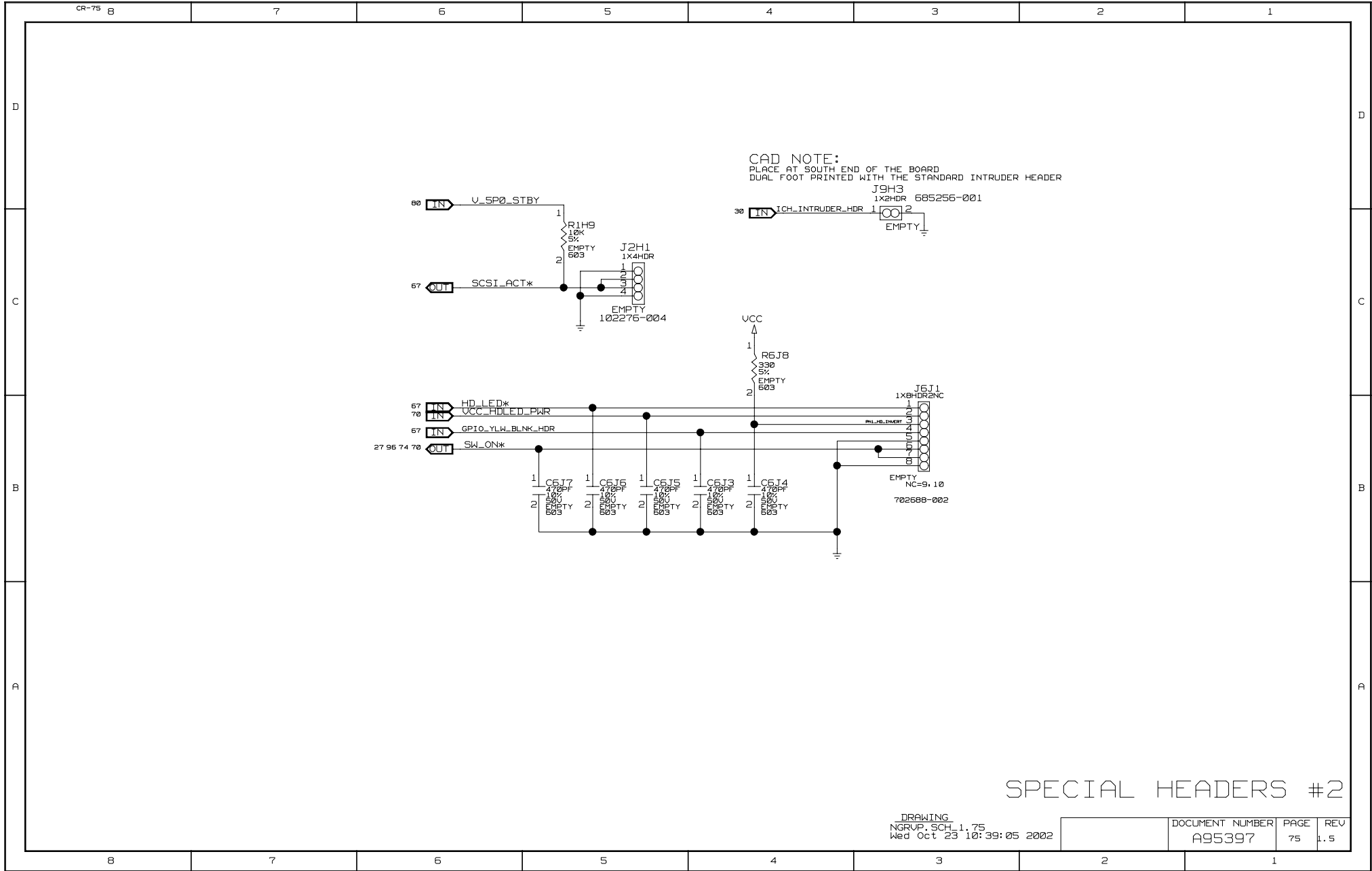
SPARES



SPECIAL HEADERS #1

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NGRUP.SCH_1.74
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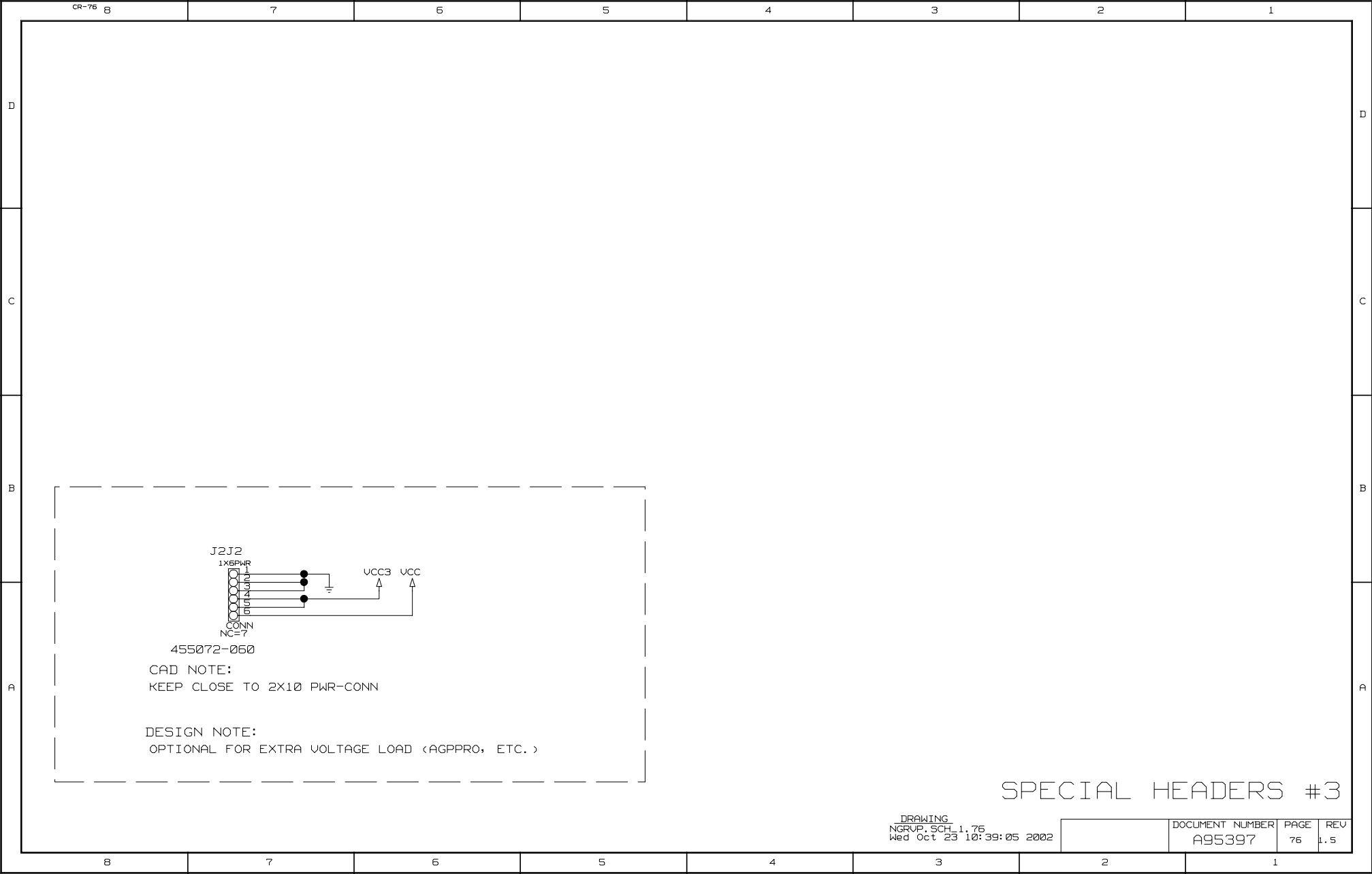
DOCUMENT NUMBER	PAGE	REV
A95397	74	1.5


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SPECIAL HEADERS #2

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 NGRUP.SCH_1.75
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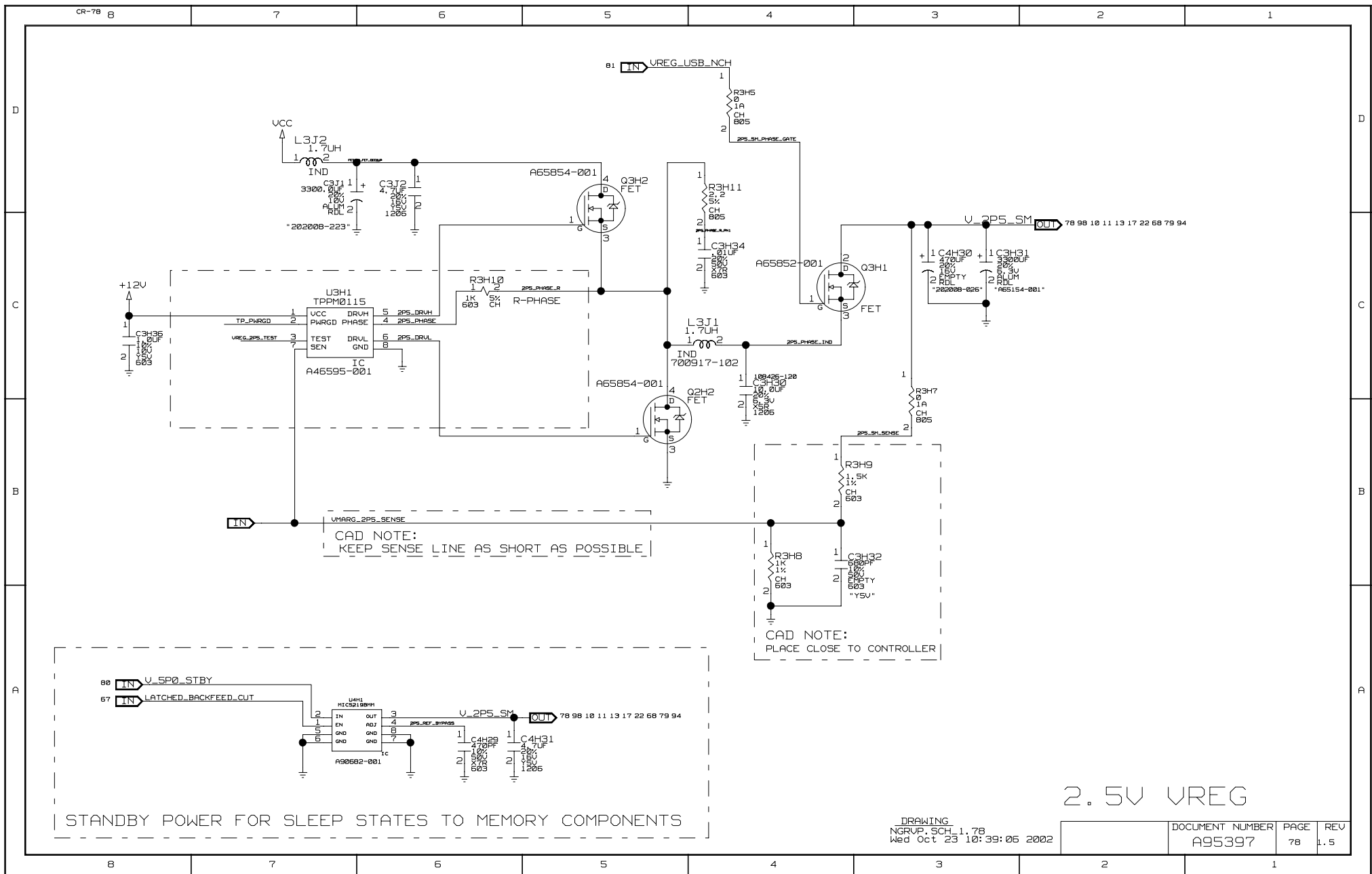
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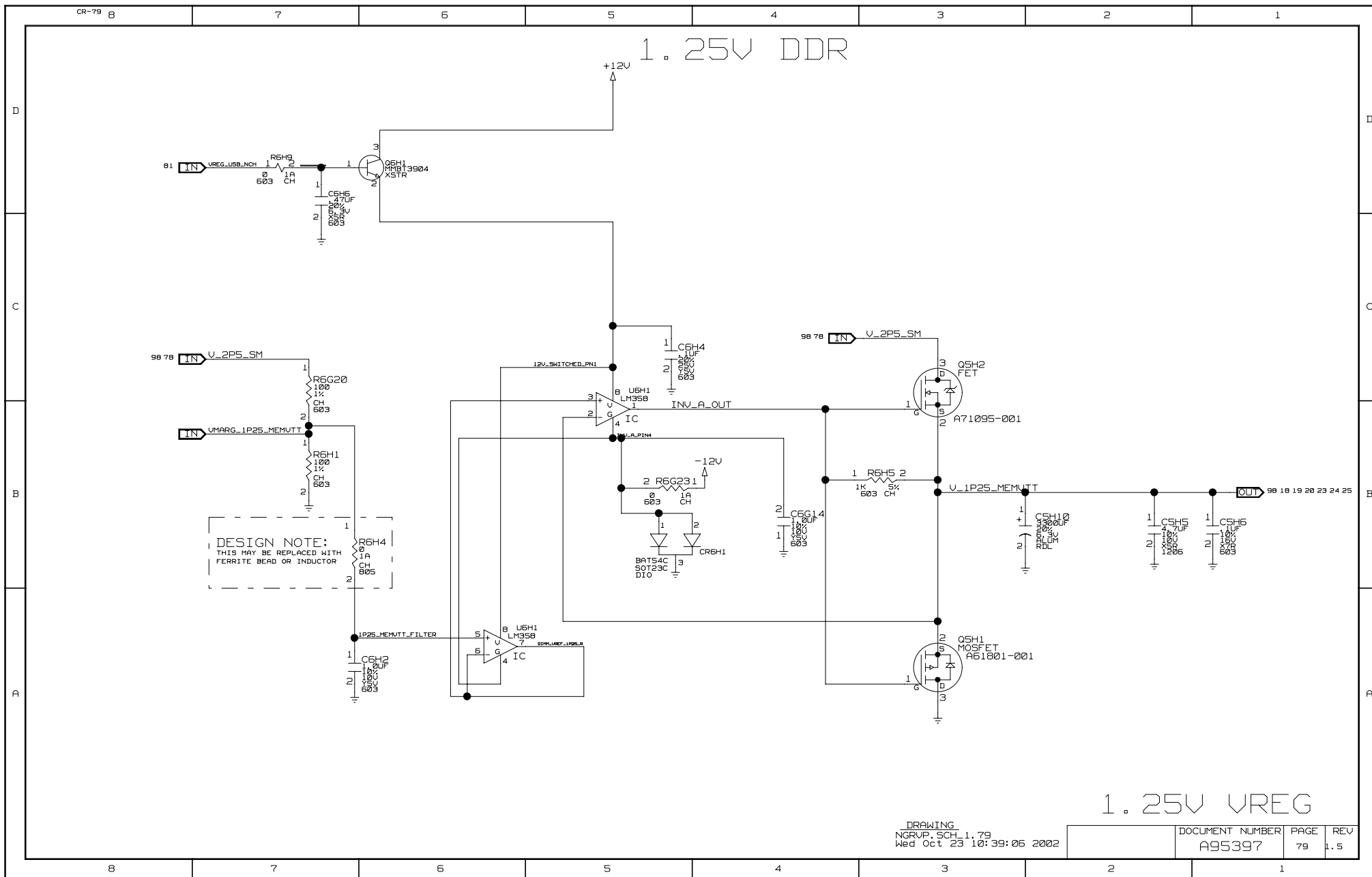


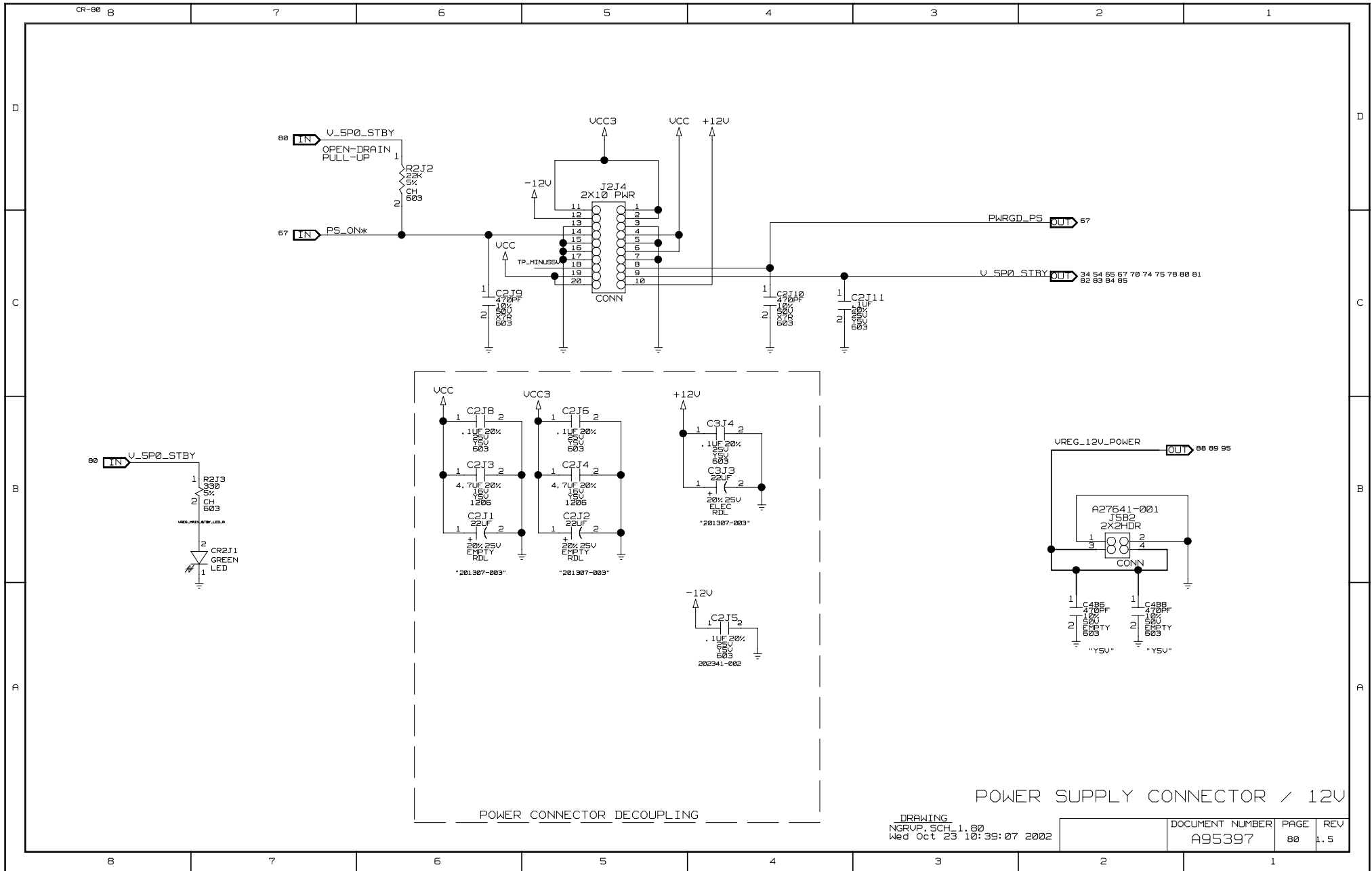
CR-77 8								7	6	5	4	3	2	1
D	E7205 MCH			FWH			HEC6							
	X.X (VCCP)			3.3 (VCC3)			3.3 STBY (VCC3 STBY)							
	1.3						5.0 (VCC)							
	1.5						12							
C	2.5			LAN			X.X (VCCP)							
	ICH			3.3 V-AUX (VCC3 OR 3.3 STBY)			2.5 (CORE)							
	X.X (VCCP)			3.3 (VCC3)										
	1.5			GLUECHIP			HEC4							
B	1.5 STBY			3.3 STBY (VCC3 STBY)			3.3 STBY (VCC3 STBY)							
	3.3 STBY (VCC3 STBY)			5.0 STBY (VCC STBY)			5.0 (VCC)							
	3.3 (VCC3)			CK-408			3.3 (VCC3)							
				CPU			X.X (VCCP)							
A	SIO (PORT ANGELES)			3.3 (VCC3)			3.3 STBY (VCC3 STBY)							
	3.3 STBY (VCC3 STBY)			5.0 STBY (VCC STBY)			X.X (VCCP)							
	SATA			1.8			2.5 (CORE)							
	1.8			3.3 (VCC3)										
	HSCOM (1394)			3.3 (VCC3)										
+12V (PLUS 12V FROM POWER-SUPPLY)														
-12V (MINUS 12V FROM POWER-SUPPLY)														
VCC3 (3.3V FROM POWER-SUPPLY)														
VCC (5.0V FROM POWER-SUPPLY)														
VCCP (1.10 - 1.85V)														
V_1P5_CORE (1.5V DERIVED FROM VCC3)														
V_1P3_CORE (1.3V DERIVED FROM VCC3)														
V_1P25_MEMVTT (1.25V DERIVED FROM V_2.5)														
V_2P5_SM (2.5V DERIVED FROM VCC)														
V_3P3_PCI_VAUX (3.3V OR 3.3-STANDBY SOURCE)														
V_1P5_STBY (1.5V DERIVED FROM 5.0-STANDBY)														
V_3P3_STBY (3.3V DERIVED FROM 5.0-STANDBY)														
V_5P0_STBY (5.0V FROM POWER-SUPPLY)														
V_3P0_BAT_VREG (~3.0V FROM THE BATTERY OR FROM 3.3STBY THROUGH A DIODE)														
V_BAT_VREG_R_CR (3.0V FROM THE BATTERY)														
VREG_12V_FILTERED (+12V FILTERED FROM 2X2 12V POWER-SUPPLY)														
VREG_USB_BP_LEFT (5.0 FROM VCCC OR 5.0-STANDBY)														
VREG_USB_BP_RIGHT (5.0 FROM VCCC OR 5.0-STANDBY)														
VREG_PS2 (5.0 FROM VCCC OR 5.0-STANDBY)														
USB_FNT_PWR (5.0 FROM VCC OR 5.0-STANDBY)														
USB_CNR_PWR (5.0 FROM VCC OR 5.0-STANDBY)														
VREG: VOLTAGE DISTRIBUTION														
VREG MAP														
DRAWING														
NGRUP: SCH 1.77														
Wed Oct 23 10:39:05 2002														
DOCUMENT NUMBER														
A95397														
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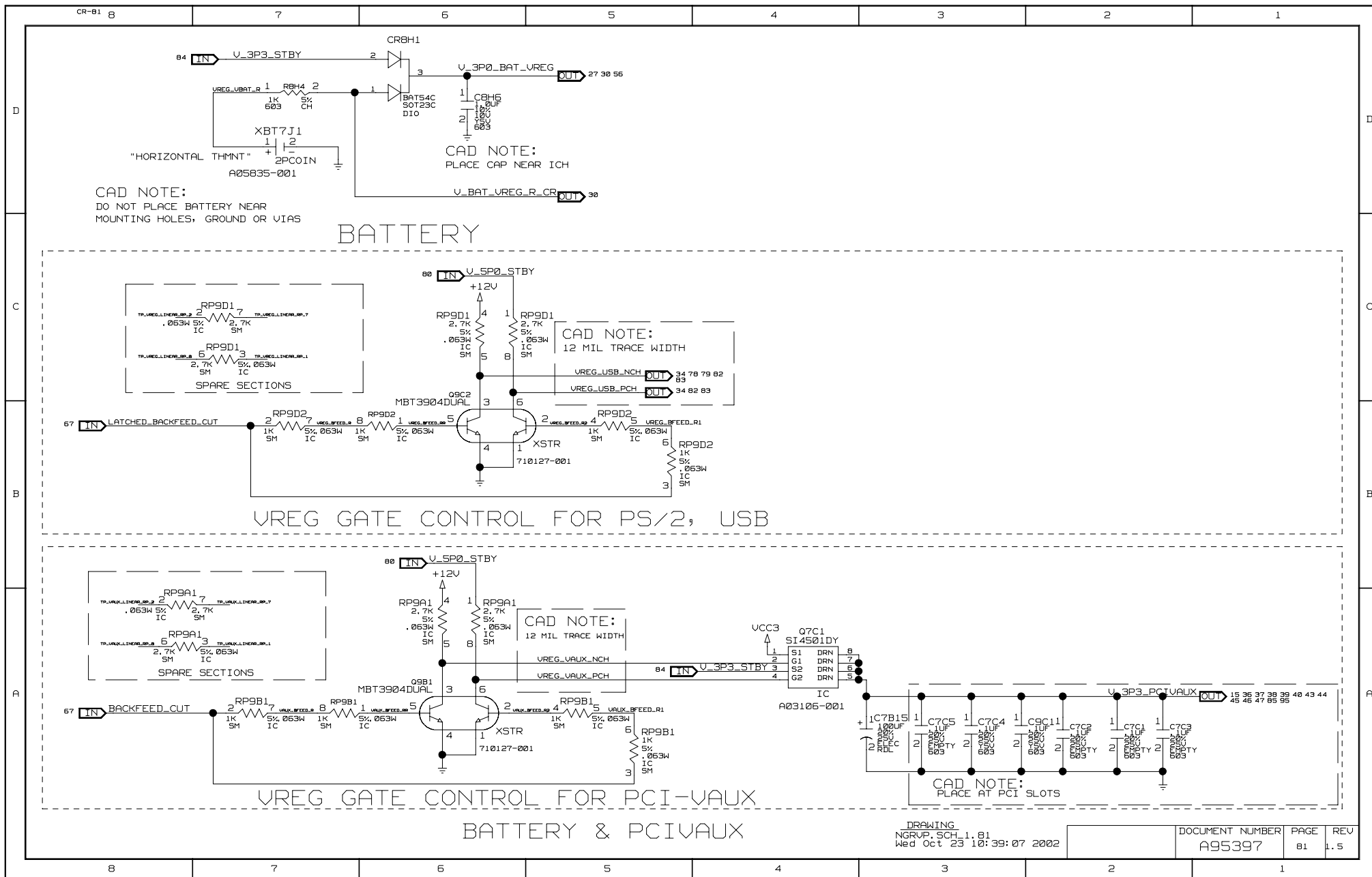
VREG: VOLTAGE DISTRIBUTION

VREG MAP









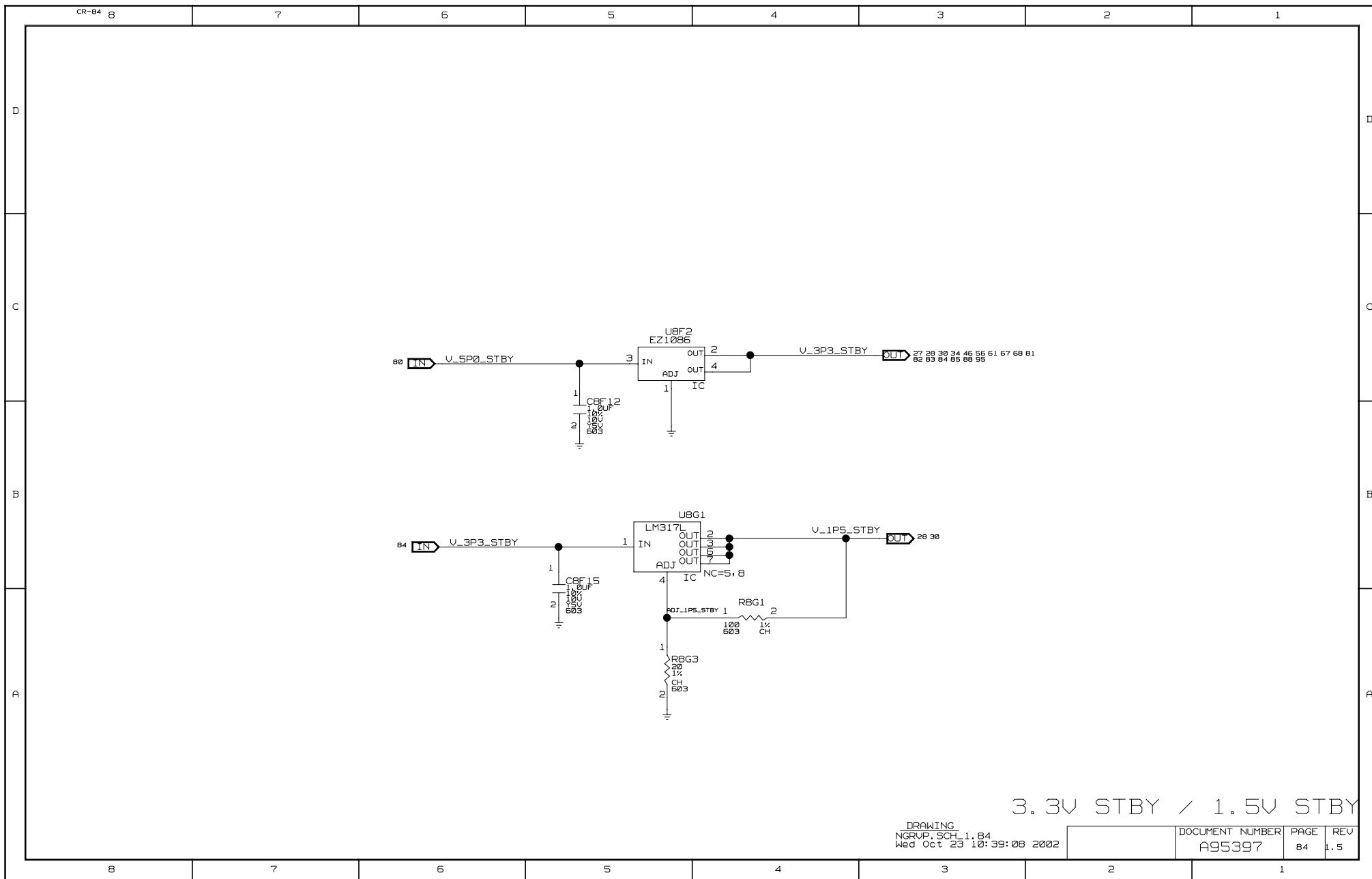


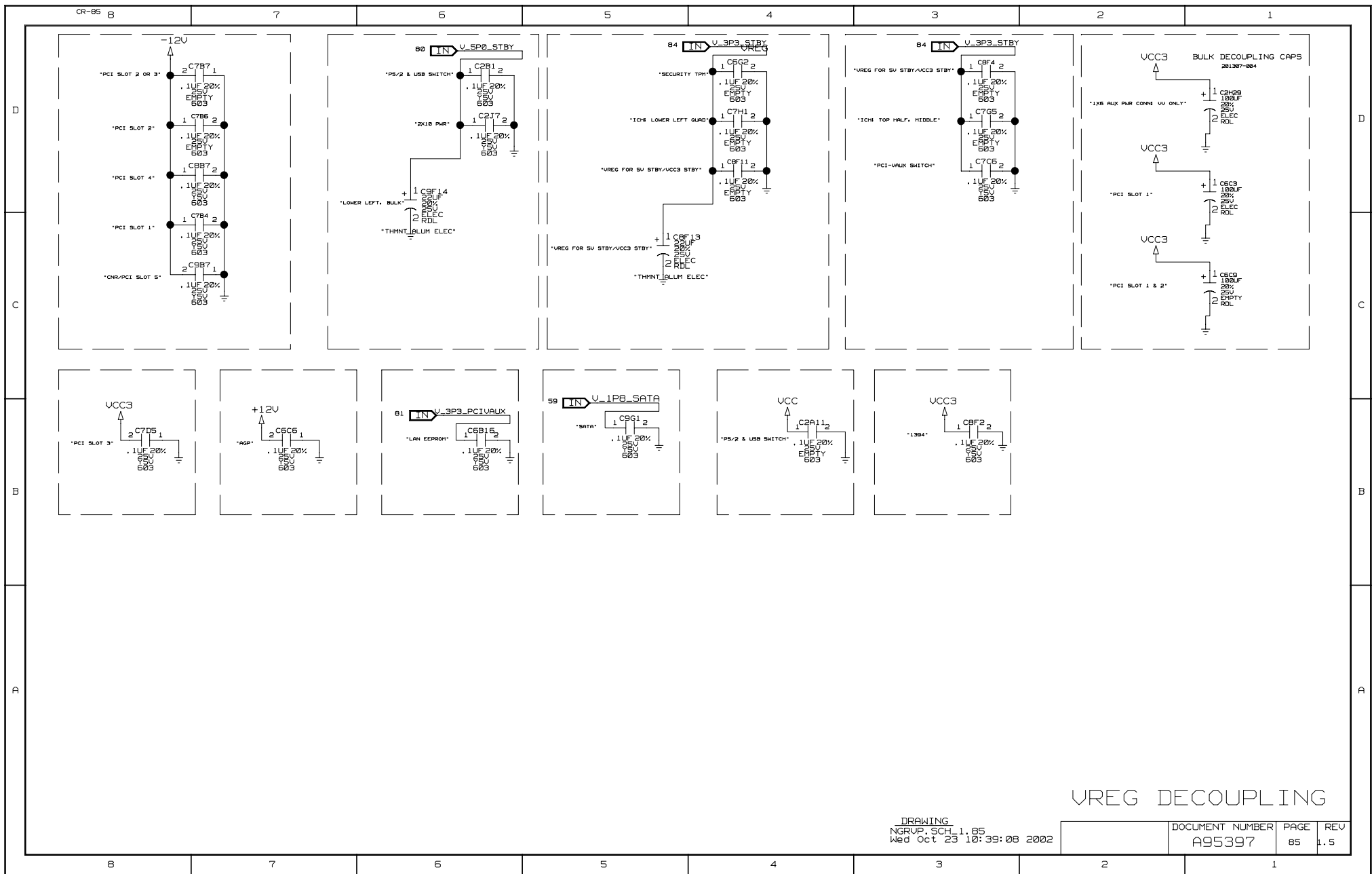
URG_USB MUST BE SPLIT
AMONGST ALL USB CHANNELS.
DO NOT DAISY CHAIN

PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR

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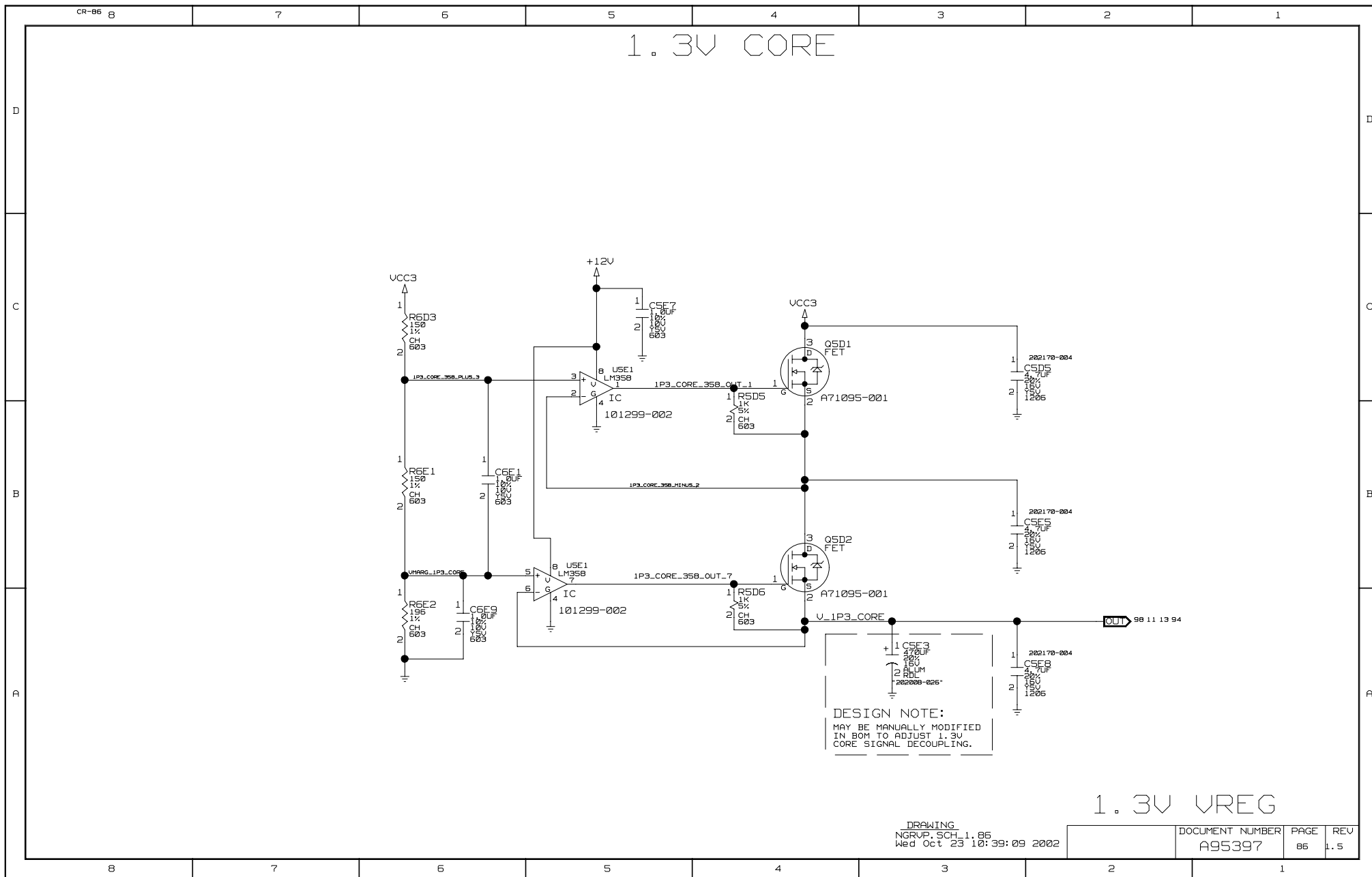


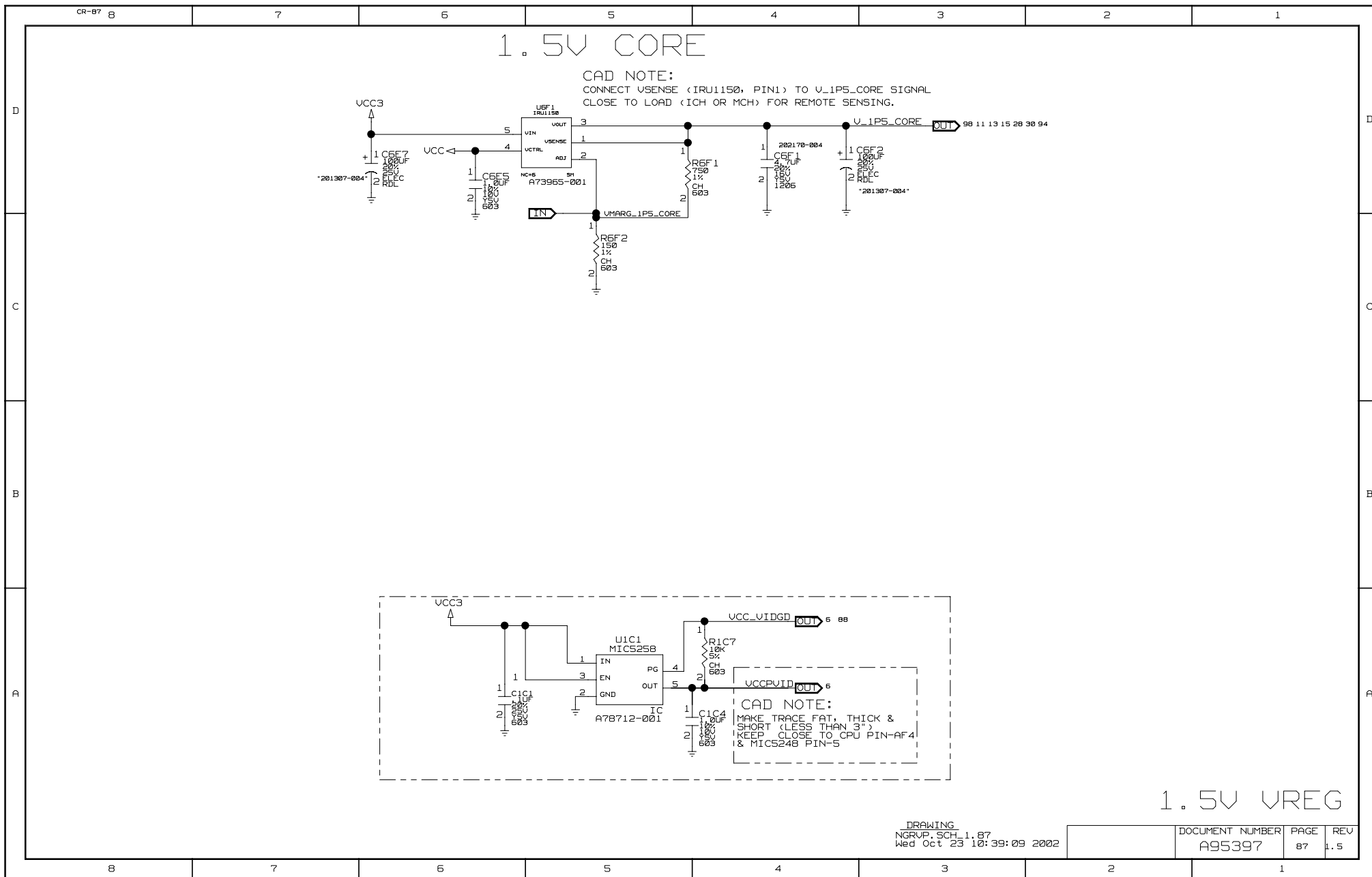


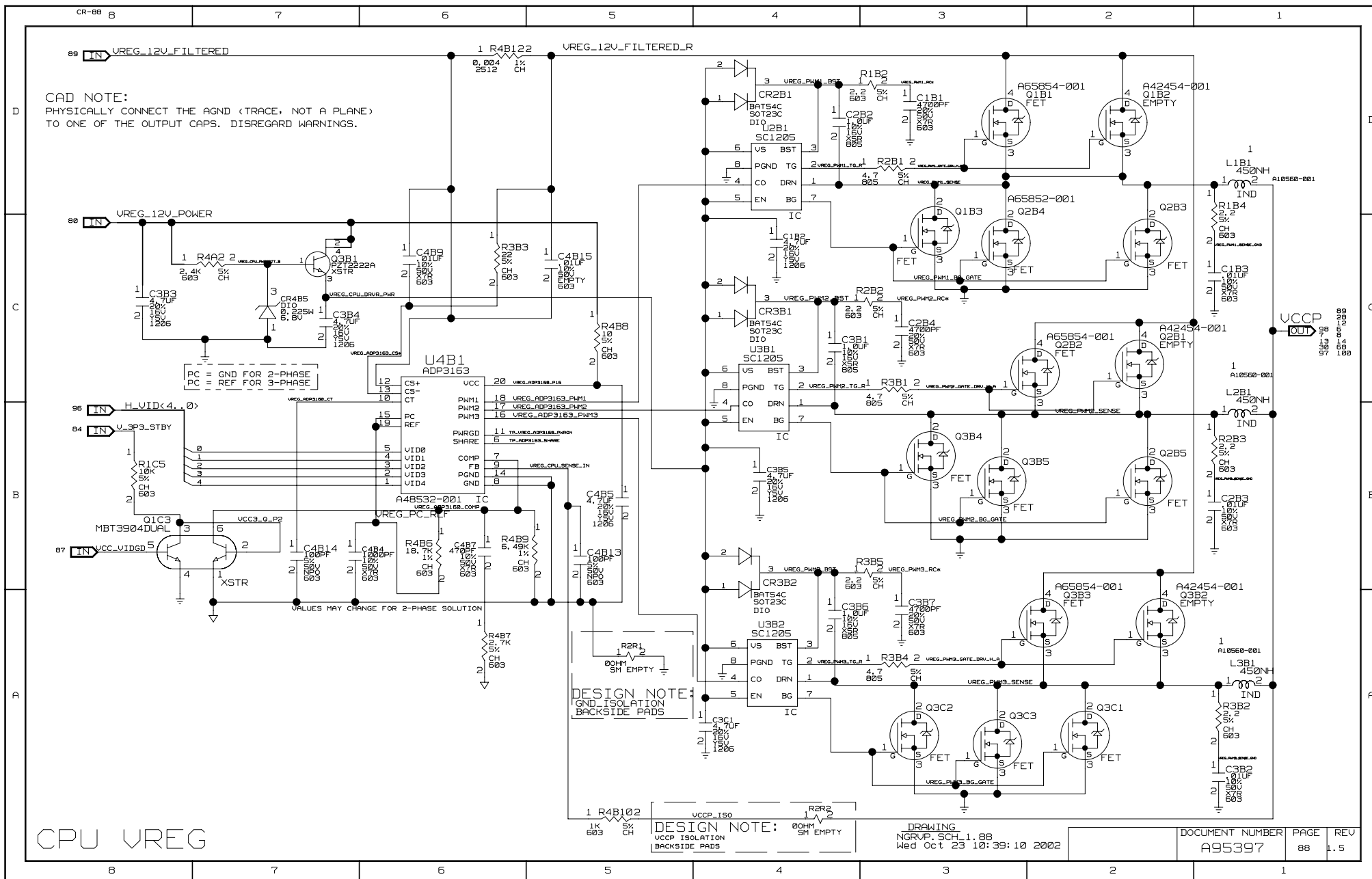
VREG DECOUPLING

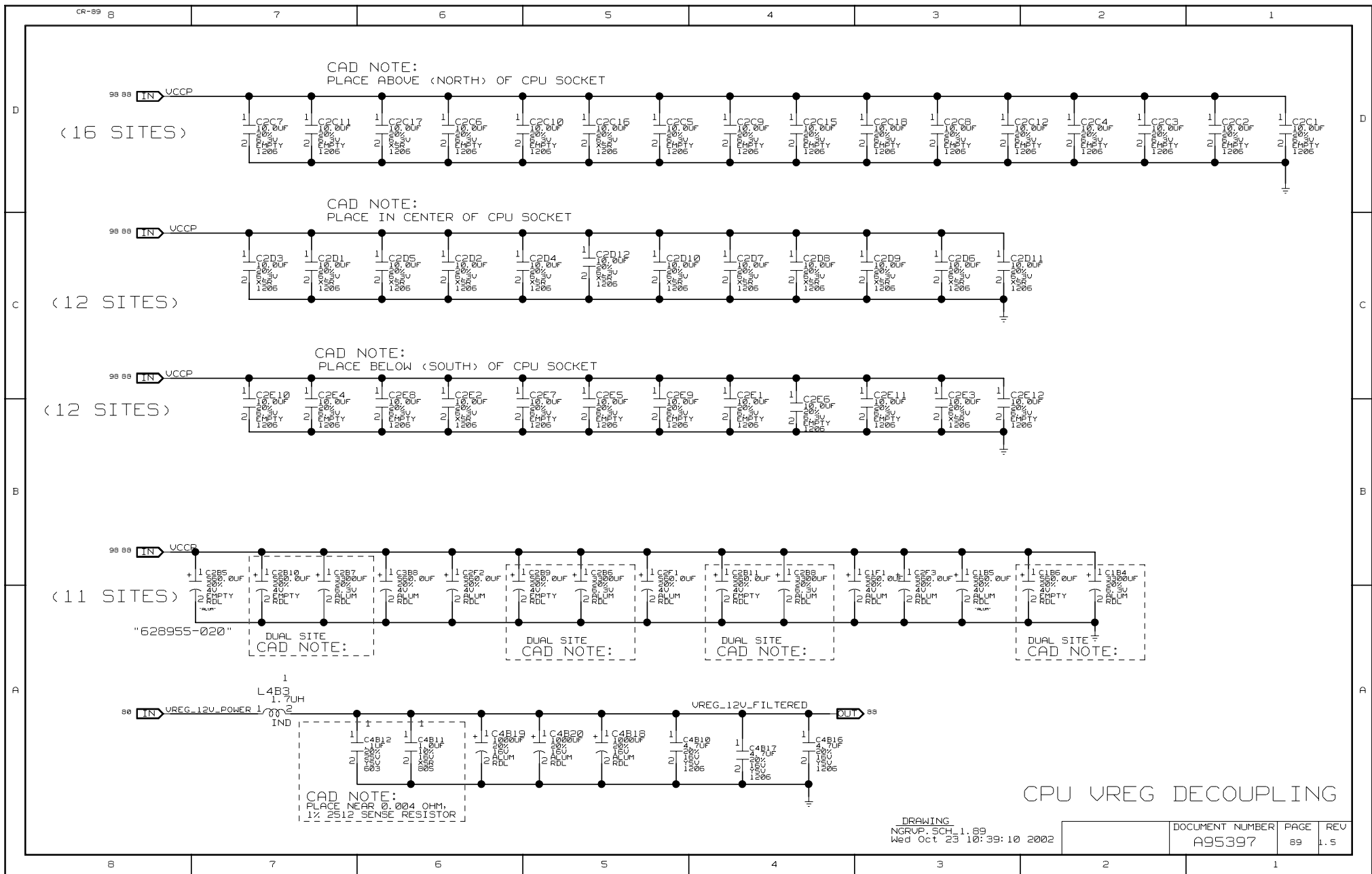
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CR-91 8

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CR-92 8

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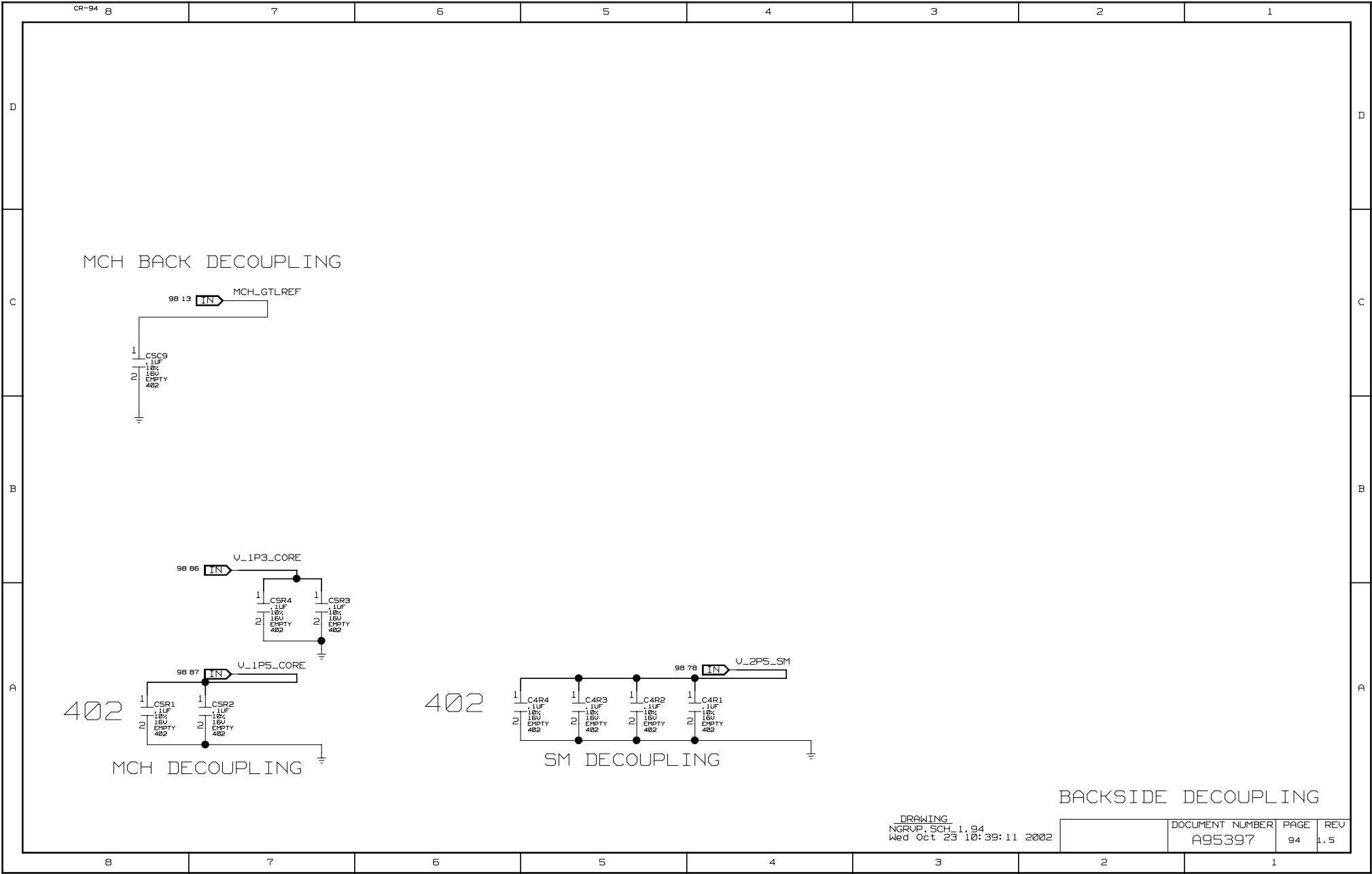
PAGE

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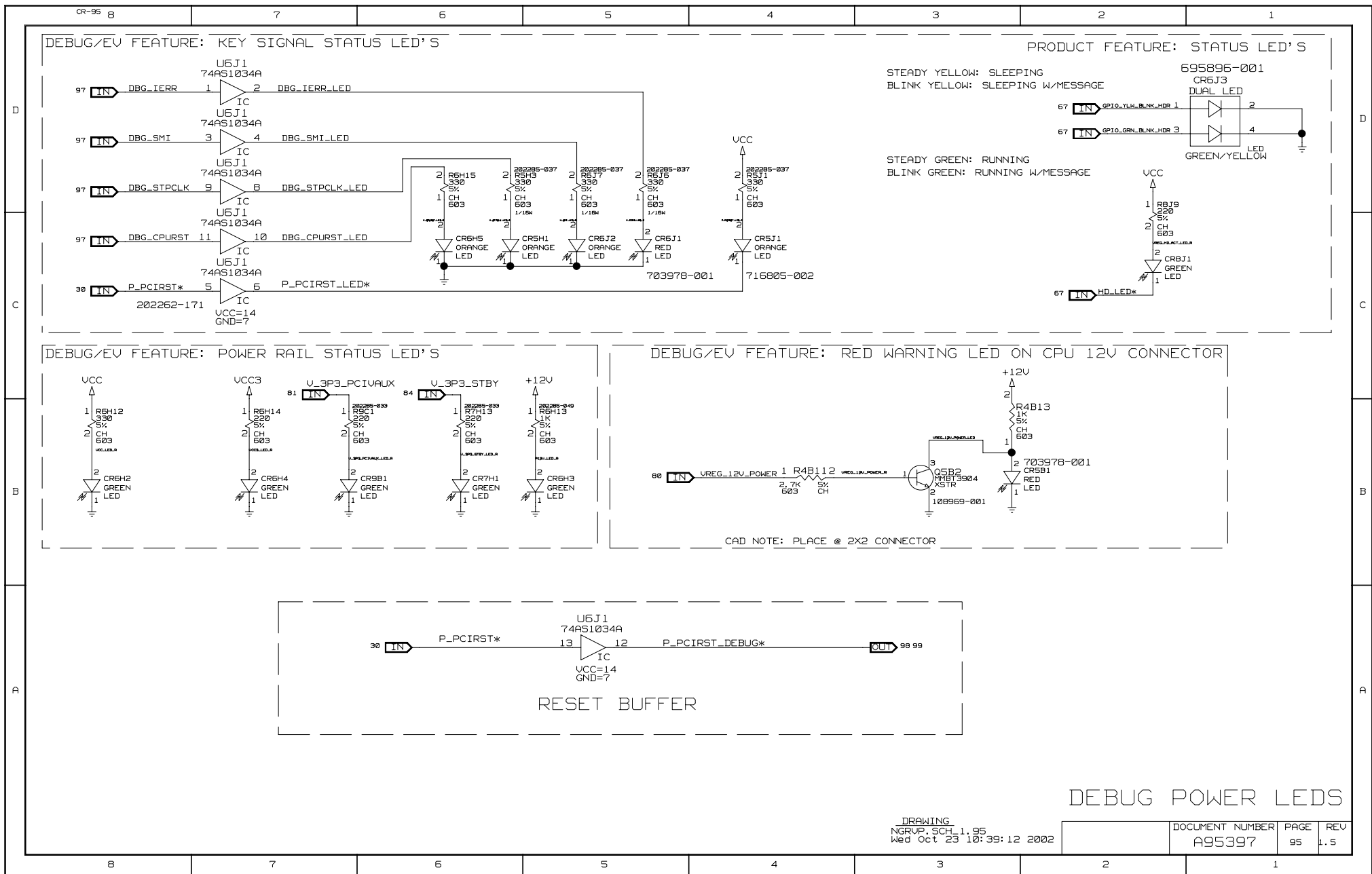
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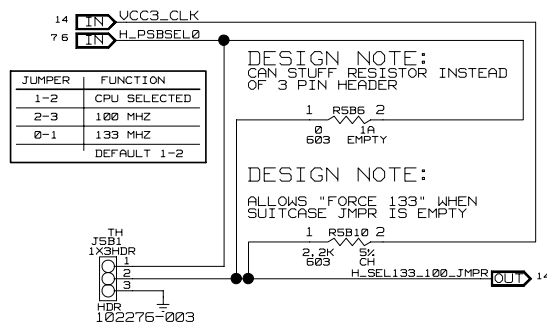
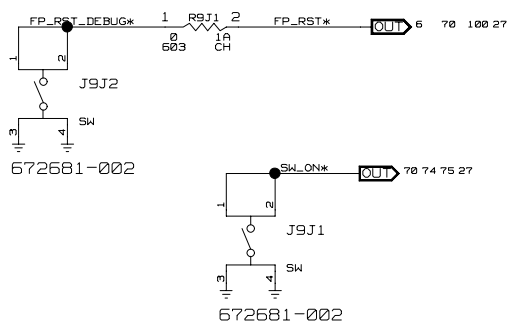
C

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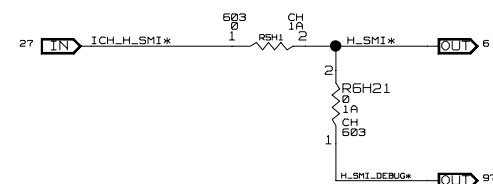
DEBUG/EV FEATURE: FRONT PANEL SWITCHES



SMI BLOCK DIAGRAM



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DEBUG/EV FEATURE: SMI LED INPUTS
```



DEBUG/EV FEATURE: VID JUMPERS

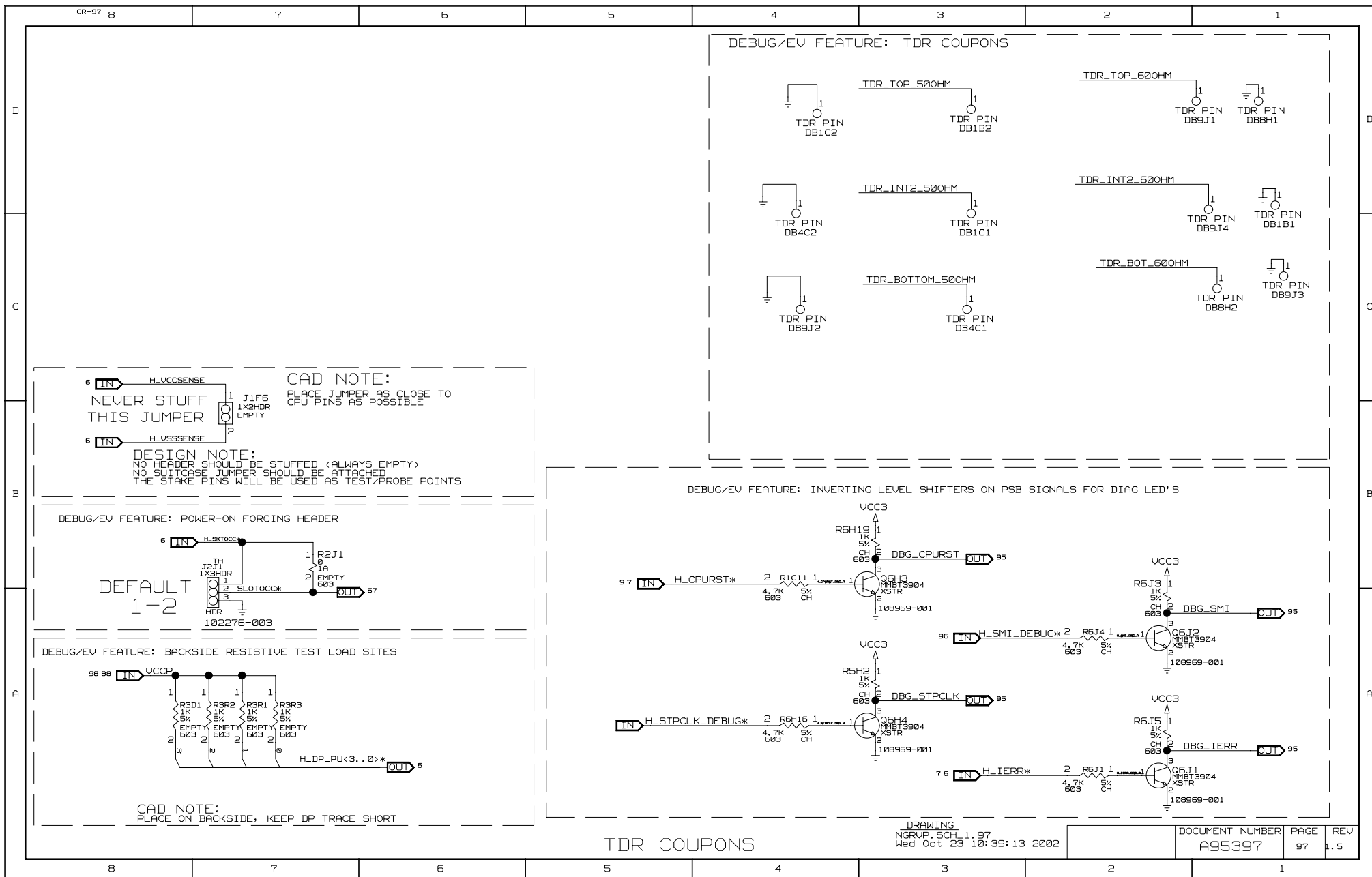
DEFAULT						
CPU DEFINED						
VID4	VID3	VID2	VID1	VID0	VOLTAGE	
1	1	1	1	1	OFF	
1	1	1	1	0	1.1	
1	1	1	0	1	1.125	
1	1	1	0	0	1.15	
1	1	0	1	1	1.175	
1	1	0	1	0	1.2	
1	1	0	0	1	1.225	
1	1	0	0	0	1.25	
1	0	1	1	1	1.275	
1	0	1	1	0	1.3	
1	0	1	0	1	1.325	
1	0	1	0	0	1.35	
1	0	0	1	1	1.375	
1	0	0	1	0	1.4	
1	0	0	0	1	1.425	
1	0	0	0	0	1.45	
0	1	1	1	1	1.475	
0	1	1	1	0	1.5	
0	1	1	0	1	1.525	
0	1	1	0	0	1.55	
0	1	0	1	1	1.575	
0	1	0	1	0	1.6	
0	1	0	0	1	1.625	
0	1	0	0	0	1.65	
0	0	1	1	1	1.675	
0	0	1	1	0	1.7	
0	0	1	0	1	1.725	
0	0	1	0	0	1.75	
0	0	0	1	1	1.775	
0	0	0	1	0	1.8	
0	0	0	0	1	1.825	
0	0	0	0	0	1.85	

* UN-DRIVEN H_VID SIGNALS WILL BE PULLED HIGH BY INTERNAL VREG RESISTOR

PWR BUTTON / VID STRAPS

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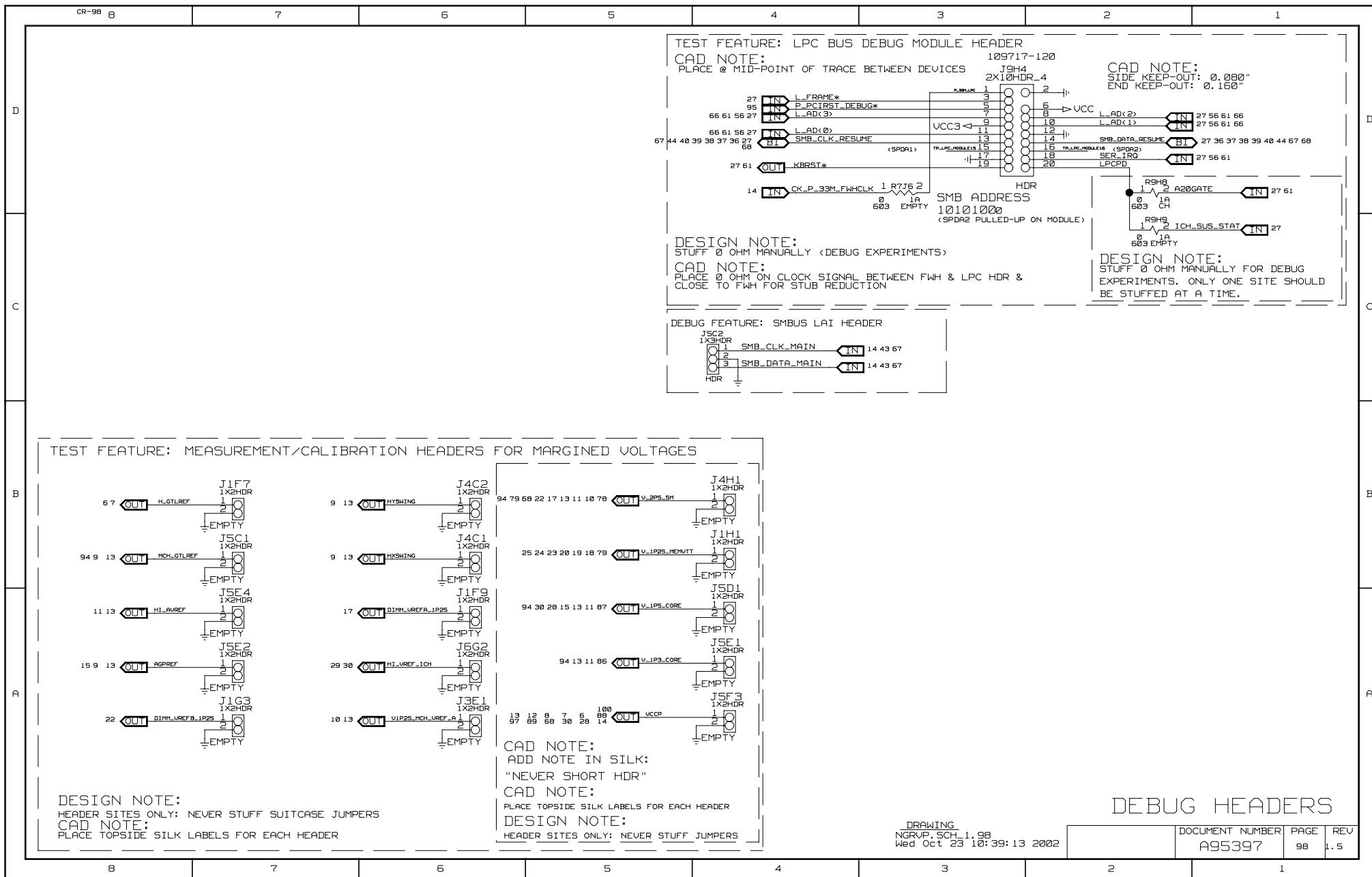
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A95397	96	1.5

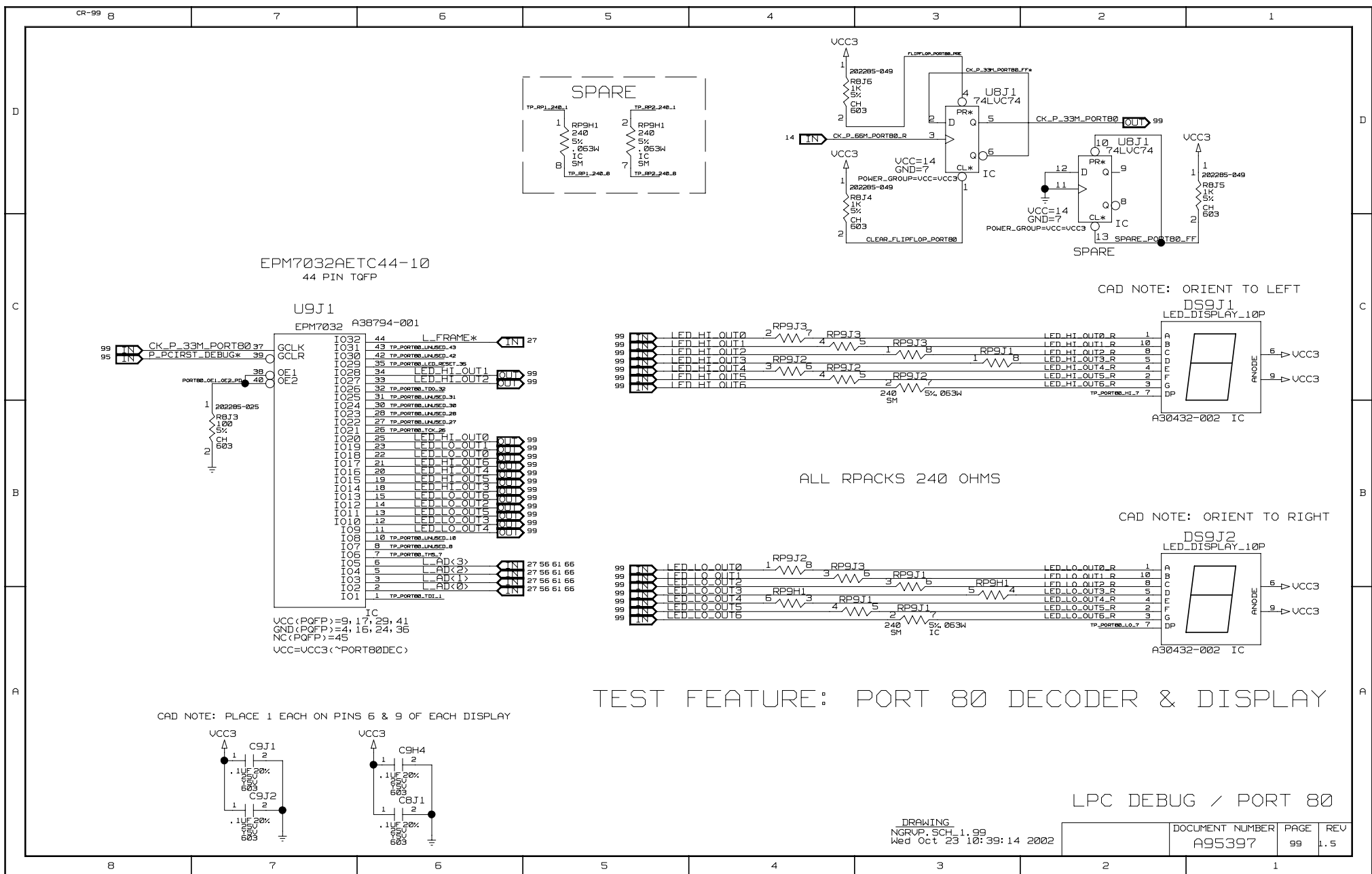


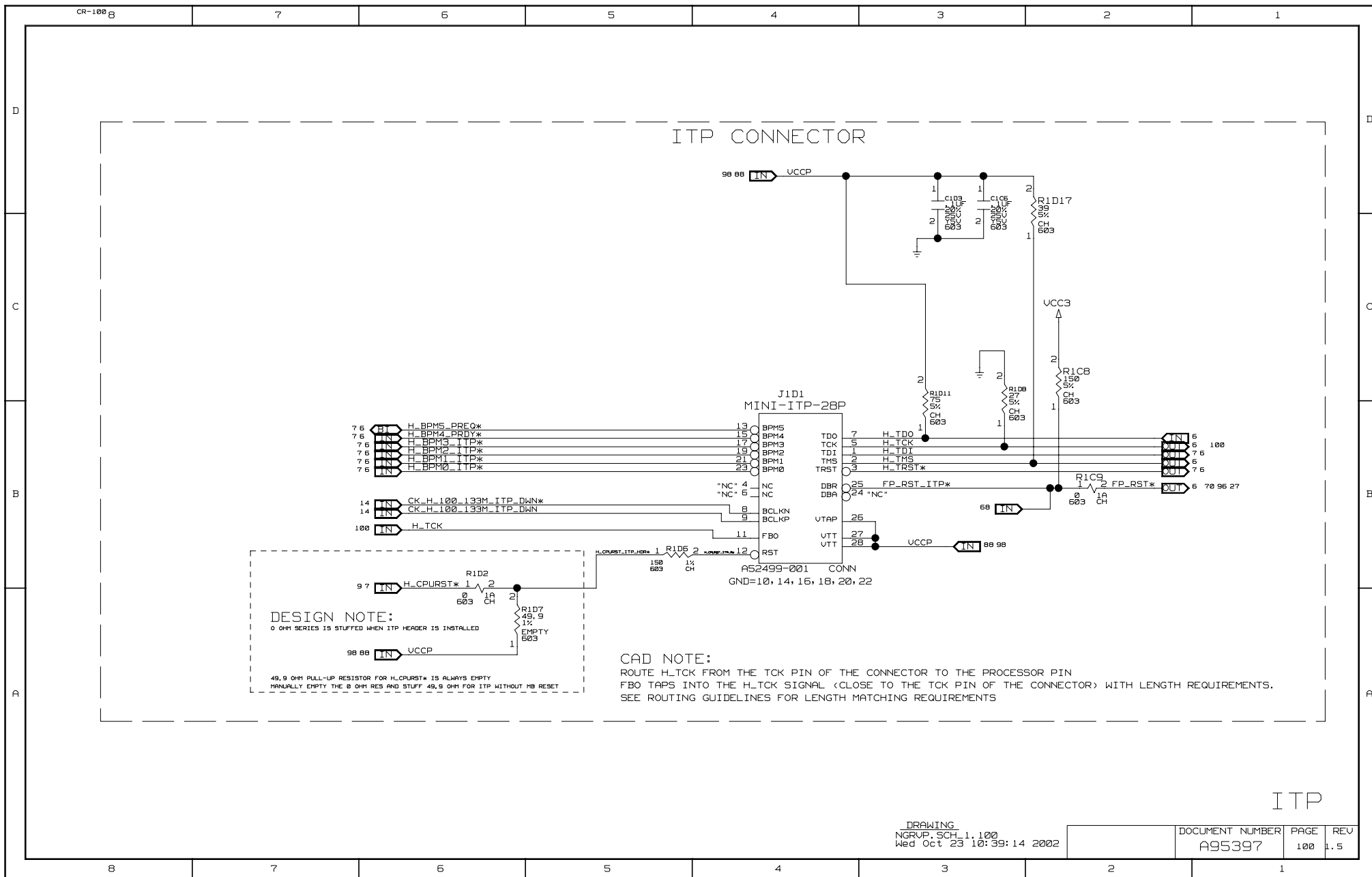
TDR COUPONS

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NGRUP.SCH_1.97
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	8	7	6	5	4	3	2	1																									
D	<p>*** Signal Cross-Reference *** --- for the entire design ---</p> <p>IP3_CORE_35B_MINUS_2 86 IP3_CORE_35B_OUT_1 86 IP3_CORE_35B_OUT_7 86 IP3_CORE_35B_PLUS_3 86 IP25_MEMORY_FILTER 79 2P5_DRVH 78 2P5_DRV_L 78 2P5_PHASE 78 2P5_PHASE_IND 78 2P5_PHASE_R 78 2P5_PHASE_R_PN1 78 2P5_REF_BYPASS 78 2P5_SH_PHASE_GATE 78 2P5_SH_SENSE 78 12V_SWITCHED_PN1 79 12V_SWITCHED_RES_XSTR_PN1 79 1394HDR3_12V_FUSE 57 1394HDRFP_12V_FUSE 57 1394HDR_12V_FUSE_57 58 1394HDR_12V_FUSE_DIO_HDR2 57 1394HDR_12V_FUSE_DIO_HDR3 57 1394HDR_12V_FUSE_DIO_PWR_9 57 1394HDR_12V_FUSE_PWR_9 57 1394HDR_DIVIDER_STRAP_0 57 1394HDR_DIVIDER_STRAP_1 57 1394HDR_DIVIDER_STRAP_2 57 1394_CLKRUN* 58 1394_CPS_PWR 58 1394_CYCLE_STRAP 58 1394_DVDD_FB 58 1394_FILTER0 58 1394_FILTER1 58 1394_GPIO_STRAP 58 1394_PHY_TEST_MA 58 1394_PLL_VDD_FB 58 1394_R0_STRAP 58 1394_R1_STRAP 58 1394_REG18A 58 1394_REG18B 58 1394_SCL 58 1394_SDA 58 1394_XTAL_X1 58 1394_XTAL_X0 58 A28GATE 27 61 98 ADJ_IP5_STBY 84 AGPREF 13 98 9 15 AGP_PRO_PRSTNT1 15 29 AGP_PRO_PRSTNT2 15 29 AGP_PSWING 13 9 APICD0_L1 30 27 AUD_3D_C 48 AUD_3D_R 48 AUD_AFLT1 48 49 AUD_AFLT2 48 49 AUD_AFLT3 48 AUD_AFLT4 48 49 AUD_A_REFFLT 48 49 AUD_A_VREF 48 55 AUD_CDC_LOUT 48 52 AUD_CDC_ROUT 48 52 AUD_CDGND 50 48 AUD_CDGND_C 50 AUD_CDGND_R 50 AUD_CK_24M_XTL_I 48 AUD_CK_24M_XTL_O 48 AUD_JACK_GND 50 51 52 54 AUD_LAUXIN 50 48</p>								<p>AUD_LAUXIN_C 50 AUD_LAUXIN_R 50 AUD_LCD 50 48 AUD_LCD_C 50 AUD_LCD_R 50 AUD_LINK_BCLK 43 48 29 AUD_LINK_BCLK_CNR 43 AUD_LINK_BCLK_R 48 AUD_LINK_RST* 29 43 48 67 AUD_LINK_SDI0 29 43 AUD_LINK_SDI0_CNR 43 AUD_LINK_SDI1 29 43 AUD_LINK_SDI2 29 43 48 AUD_LINK_SDI2_R 48 AUD_LINK_SDO 30 43 48 AUD_LINK_SDO_CNR 43 AUD_LINK_SDO_R 29 30 66 AUD_LINK_SYNC 30 43 48 AUD_LINK_SYNC_CNR 43 AUD_LINK_SYNC_R 29 30 AUD_LLINEIN 50 48 AUD_LLINEIN_C 50 AUD_LLINEIN_R 50 AUD_LLINEIN_R_FB 50 51 AUD_L_FINTOUT 52 53 AUD_L_LINEOUT 52 AUD_L_LINEOUT_FB_PN1 52 AUD_L_PCSPKR 52 55 AUD_L_RETIN 52 53 55 AUD_MICIN_AMP_MINUS 51 AUD_MICIN_AMP_PLUS 51 AUD_MICIN_AMP_PLUS_PN 51 AUD_MICIN_AMP_PLUS_R 51 AUD_MIC_BIAS 51 53 AUD_MIC_BIAS_R 51 AUD_MIC_BIAS_REF 51 AUD_MIC_IN 51 48 AUD_MIC_IN_AMP_OUT_PN1 51 AUD_MIC_IN_AMP_OUT_PN2 51 AUD_MIC_IN_FP 53 51 AUD_MIC_IN_FP_PN1 51 AUD_MIC_OUT_PN1 51 AUD_MONO_IN 50 48 AUD_MONO_IN_PN1 48 AUD_MONO_IN_R 48 AUD_MONO_OUT_C 48 50 AUD_MONO_OUT_C_HDR 50 AUD_PCBECP_IN_CODEC 48 AUD_RAUXIN 50 48 AUD_RAUXIN_C 50 AUD_RAUXIN_R 50 AUD_RCD 50 48 AUD_RCD_C 50 AUD_RCD_R 50 AUD_RLINEIN 50 48 AUD_RLINEIN_C 50 AUD_RLINEIN_R 50 AUD_RLINEIN_R_FB 50 AUD_R_FINTOUT 52 53 AUD_R_LINEOUT 52 AUD_R_LINEOUT_FB_PN1 52 AUD_R_PCSPKR 52 55 AUD_R_RETIN 52 53 55 AUD_SPDIF 48 52 AUD_SPDIF_LEFT 52 AUD_SPDIF_XSTR 55 AUD_SPDIF_XSTR1_VCC 55 AUD_SPDIF_XSTR2_VCC 55 AUD_SPDIF_XSTR3_VCC 55 AUD_SPK_AMP_NEG_OUT 55</p>								<p>AUD_SPK_AMP_P3 55 AUD_SPK_AMP_P4 55 AUD_SPK_AMP_POS_OUT 55 AUD_STRAP_45 48 AUD_STRAP_46 48 AUD_VREF_FDBK 55 AUD_VREF_IN 55 AUD_VREF_OUT 55 AUD33_ANALOG_R 48 AVSS2_DCPL 48 AVSS3_GNDSTRAP 48 BACKFEED_CUT 67 81 BOARDID(4, 0) 30 29 CDC_DWN_ENAB* 30 43 67 27 CDC_DWN_RST* 67 48 CDC_RESET* 48 CK_14M_AUD 14 48 CK_14M_ICH 14 27 CK_14M_SIO 14 61 CK_14M_SIO_ICH_R 14 CK_48M_ICH_USB 14 29 CK_48M_ICH_USB_R 14 CK_48M_SIO_USB 14 CK_48M_SIO_USB_R 14 CK_66M_MCH 14 9 CK_66M_MCH_R 14 CK_CPU_PCI_STOP 14 CK_G_66M_AGP 14 15 CK_G_66M_AGP_R 14 CK_HBL_66M_ICH 14 29 CK_HBL_66M_ICH_R 14 CK_H_100_133M_CPU 14 6 CK_H_100_133M_CPU* 14 6 CK_H_100_133M_CPU_R 14 CK_H_100_133M_CPU_R* 14 CK_H_100_133M_I7P_CPU 14 6 CK_H_100_133M_I7P_CPU* 14 6 CK_H_100_133M_I7P_DWN 14 100 CK_H_100_133M_I7P_DWN* 14 100 CK_H_100_133M_I7P_PN1 14 CK_H_100_133M_I7P_PN1* 14 CK_H_100_133M_I7P_R 14 CK_H_100_133M_I7P_R* 14 CK_H_100_133M_MCH 14 9 CK_H_100_133M_MCH* 14 9 CK_H_100_133M_MCH_R 14 CK_H_100_133M_MCH_R* 14 CK_MULT0 14 CK_M_133M_N_DDR0_A 10 17 CK_M_133M_N_DDR0_B 10 22 CK_M_133M_N_DDR1_A 10 17 CK_M_133M_N_DDR1_B 10 22 CK_M_133M_N_DDR4_A 10 17 CK_M_133M_N_DDR4_B 10 22 CK_M_133M_N_DDR5_A 10 17 CK_M_133M_N_DDR5_B 10 22 CK_M_133M_N_DDR6_A 10 17 CK_M_133M_N_DDR6_B 10 22 CK_M_133M_P_DDR0_B 10 22 CK_M_133M_P_DDR1_A 10 17 CK_M_133M_P_DDR1_B 10 22 CK_M_133M_P_DDR4_A 10 17 CK_M_133M_P_DDR4_B 10 22 CK_M_133M_P_DDR5_A 10 17 CK_M_133M_P_DDR5_B 10 22 CK_M_133M_P_DDR6_A 10 17 CK_M_133M_P_DDR6_B 10 22</p>								<p>CK_M_133M_P_DDR7_A 10 17 CK_M_133M_P_DDR7_B 10 22 CK_P_33M_1394 14 58 CK_P_33M_1394_SATA_R 14 CK_P_33M_ARB 14 42 CK_P_33M_FWHCLK 14 66 98 CK_P_33M_ICH 14 26 CK_P_33M_ICH_R 14 CK_P_33M_LAN 14 44 CK_P_33M_LAN_R 14 CK_P_33M_PORTB0 99 CK_P_33M_PORTB0_FF* 99 CK_P_33M_S1 14 48 CK_P_33M_S1_R 14 CK_P_33M_S2 14 39 CK_P_33M_S2_R 14 CK_P_33M_S3 14 38 CK_P_33M_S3_R 14 CK_P_33M_S4 14 37 CK_P_33M_S4_R 14 CK_P_33M_S5 14 36 CK_P_33M_S5_R 14 CK_P_33M_SATA 14 58 CK_P_33M_SIO 14 61 CK_P_33M_SIO_R 14 CK_P_33M_TPM 14 56 CK_P_33M_TPM_FWH_R 14 CK_P_66M_PORTB0_CLK_R 14 CK_P_66M_PORTB0_R 14 99 CLEAR_FLIPFLOP_PORTB0 99 CLK_IREF 14 CNR_SMB_A0 43 CNR_SMB_A1 43 CNR_SMB_A2 43 CORE_SPKR_R 69 CPU_DRIVER 72 CPU_FAN_PWM 61 68 72 CPU_FAN_TACH 72 68 CPU_TACH_OUT 72 DBG_CPURST 97 95 DBG_CPURST_LED 95 DBG_IERR 97 95 DBG_IERR_LED 95 DBG_SMI 97 95 DBG_SMI_LED 95 DBG_STPCLK 97 95 DBG_STPCLK_LED 95 DIMM_VREFB_IP25 17 98 17 DIMM_VREFB_IP25 22 98 22 DIMM_VREF_IP25_R 79 DRCOMPREF_H_U 13 10 DRCOMP_H 13 10 DRCOMP_U 13 10 EEPROM_ORG_ICH 46 EEPROM_ORG_LAN 46 EMAIL_BUF2 74 EMAIL_BUF_P4 74 EMAIL_LED 74 FAN1_TACH 61 FAN2_TACH 61 FET_TO_FET_DECOUP 78 FLIPFLOP_PORTB0_PRE 99 FNT_REAR_FAN_PWM3 61 68 72 FNT_REAR_FAN_PWM3_PN1 72 FNT_REAR_FAN_PWM3_XSTR 72 FP_RST* 6 70 96 100 27 FP_RST_DEBUG* 96 FP_RST_I7P* 68 100 FRONT_DRIVER 72 FRONT_FAN_PWM_R 72</p>								
C																																	
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